2. BASIC NODE

2.1 Introduction

The DXX Basic Node is a 64 Mbit/s flexible cross-connection device. There are two different types of Basic Nodes available:

— 6U high 19-inch single subrack node (RXS-S) or
— 13U high 19-inch double subrack node (RXS-D)

A DXX Double Basic Node contains two shelves connected via a bus extension from the upper shelf.

A DXX Single Basic Node contains one shelf that mounts into a standard 19" relay rack.

Basic Node has some common parts which are found in every Basic Node. These are power supply, control unit and cross-connect unit. Any free slot can be filled with different kinds of base units and interface modules.

2.2 General

2.2.1 Node Structure

The Basic Node consists of:

— common units (subrack, power/fuse unit, control unit and cross-connect unit)
— interface units (selected according to applications)

The block diagram of a node is shown in Fig. 1. An equipped single subrack is presented in Fig. 2.

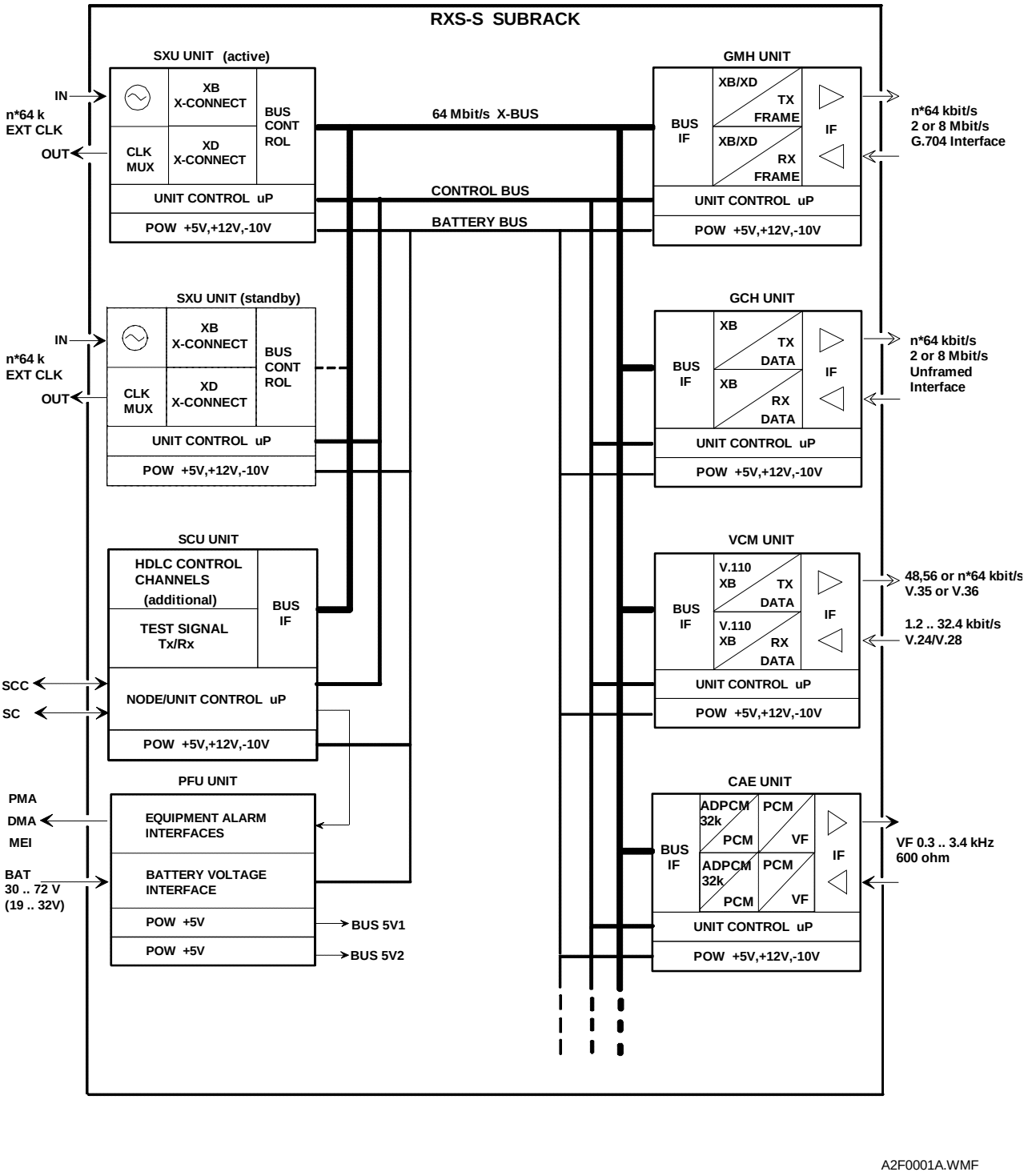


Fig. 1: Node Block Diagram

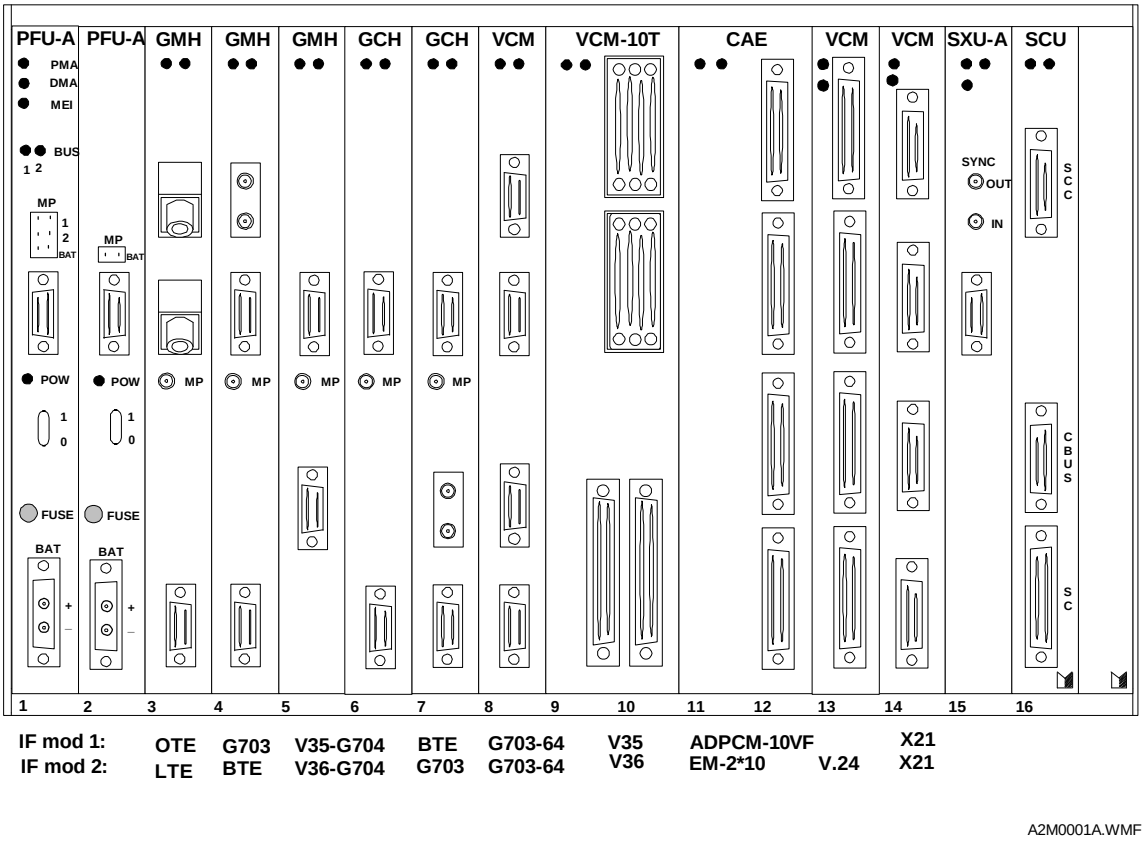


Fig. 2: An Equipped Single Subrack Node

There are two common logic units in the Basic Node. These units are the SCU and the SXU.

The SCU is the DXX node's master unit. SCU's responsibility is to communicate with the NMS computer and with the local service computer. It maintains the unit list of the node, supervizes and informs about the faults of the node and performs the change-over of SXU's when the cross-connection is protected. The test transmitter and receiver resides in the SCU unit.

The SXU is the DXX node's cross-connect unit. It performs the cross-connections, controls the cross-connect bus and selects the reference signal for the master clock oscillator. The node's master clock oscillator resides in the SXU unit.

2.2.2 Node Equipping

The card slots in the single subrack are numbered from 1 to 16 (see Fig. 3). The fuse unit, the control unit and the cross-connect unit all have fixed card slots in the subrack. The single subrack node has 9…13 slots for interface units (depending on the use of PFU unit, PFU protection, SXU type and SXU protection). The double subrack node has 23…28 slots for interface units. The interface units can be freely positioned in these card slots except that a GMH unit with an active HDLC link (trunk or NTU-A) cannot be in the last slot (32) of the double subrack. A 5T IF unit can be placed in any card slot from 2 to 14 (upper shelf) and 2 to 16 in the lower shelf. A 10T IF unit reserves two slots.

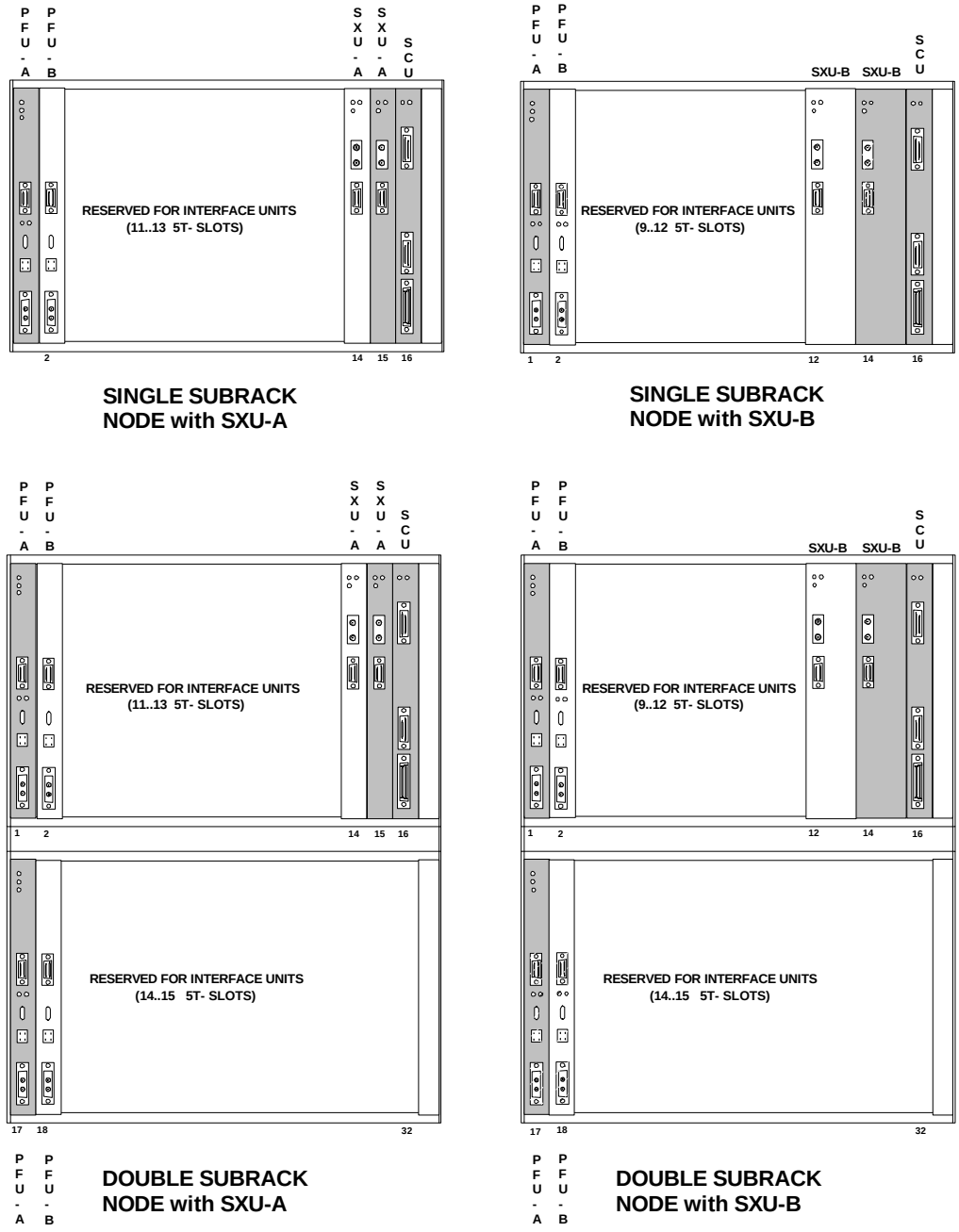


Fig. 3: Main Units and Interface Unit Slots in Single and Double Subrack Node

2.3 SCU Control Unit

2.3.1 General

The structure of the SCU unit is based on the standard mechanics of the DXX system. The width of the unit is 5T or one card slot in DXX subrack. Card slot 16 (on the upper shelf of a double subrack node) is reserved for the SCU unit.

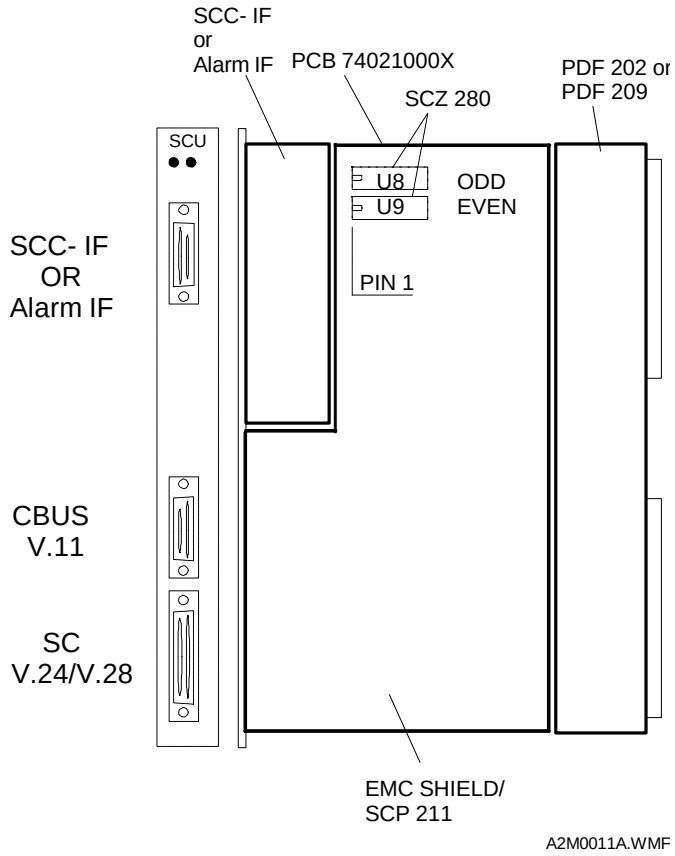


Fig. 4: SCU Unit Equipped with SCC-IF/ALARM-IF

The SCU unit needs to operate one piggy-back power supply unit PDF 202 or PDF 209 and two EPROMs with SCZ 280 program. The SCC X.25 interface module SCC-IF and the control channel expansion module HDLC-4CH (SCP 211 in Fig. 4) are options which can be installed in the same way as a normal interface piggy-back module of the DXX system. The alarm interface module ALARM-IF can be installed in the place of the SCC-IF.

Starting from the upper edge of the front panel of the unit, there are two alarm LEDs, one SCC connector, one CBUS connector and, as the lowest, the SC connector. On the back side of the unit there are two 2 x 32 pin eurocard (DIN 41612) connectors. The upper connector is used in transmitting the LOCAL VTP bus signals, equipment alarm output signals, 5 V power to the bus interface circuits and test input/output signals. The lower connector is used in transmitting the cross-connect bus signals, the 5 V power to the bus interface circuits and the battery bus.

2.3.2 SCU Operation

2.3.2.1 General

The main functions of the SCU unit are the power supply, microprocessor with its auxiliary circuits, the test signal Tx/Rx generator inside of the IFMOD ASIC, the additional HDLC control channels option and the cross-connect bus interface.

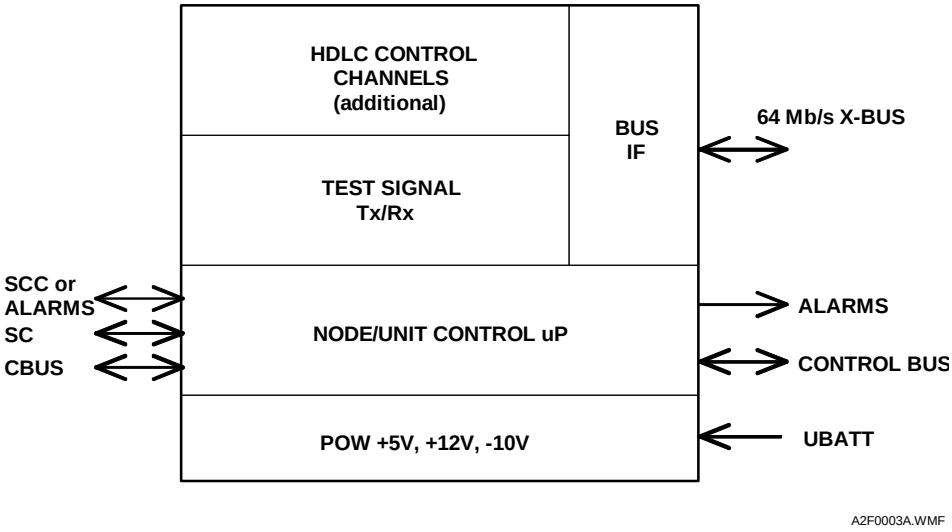


Fig. 5: SCU Block Diagram

The power supply delivers the operating voltages of the SCU unit from the battery bus voltage. The operating voltages are monitored by the microprocessor and if there is a failure, an alarm message is generated.

The detailed block diagram of the node/unit control block shows how the microprocessor controls and monitors the operation of the unit.

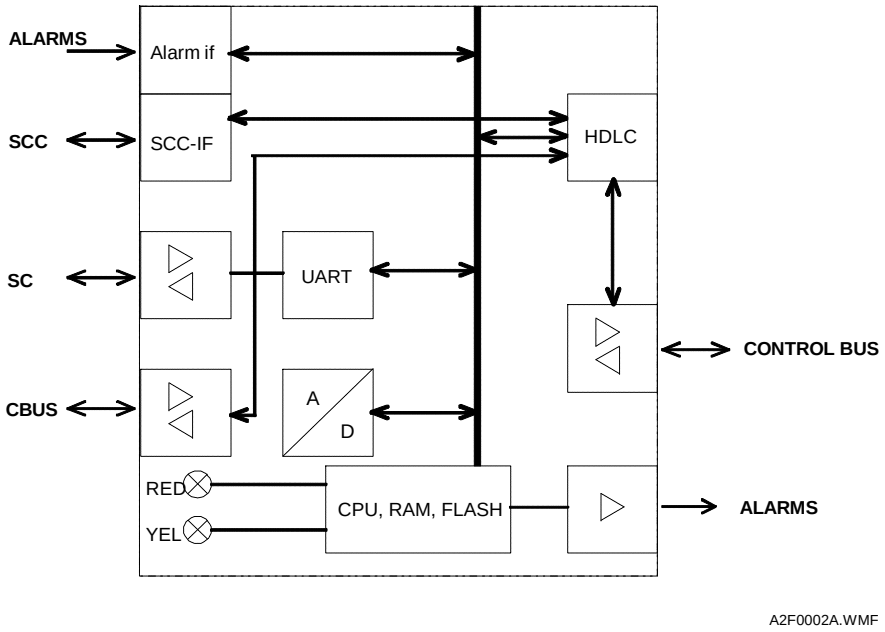


Fig. 6: Node/Unit Control microprocessor

2.3.2.2 Unit Controller

The microprocessor of the SCU unit is a 16-bit CMOS 80C186-16. It has three internal timers, two DMA channels; an interrupt controller; programmable memory and peripheral chip select logic; programmable wait state generator and local bus controller. It supports system-level testing (ONCE test mode).

The microprocessor is upward compatible with 8086 and 8088 software and fully compatible with 80186 and 80188 software. The microprocessor has two major modes of operation: compatible and enhanced. In compatible mode the microprocessor is completely compatible with NMOS 80186, with the exception of 8087 support. The features of the enhanced mode are power-save control, dynamic RAM refresh and an asynchronous numeric coprocessor interface. The enhanced mode is used in the SCU unit.

2.3.2.3 Memory

Memory is implemented with six 32-pin surface mount components providing:

— 256 kBytes RAM (U15, 16)
— 512 kBytes FLASH PROM in two banks (U10, 11, 12 and 13)
— 256 kBytes of EPROM in two DIP packages (U8, 9)

2.3.2.4 HDLC Channels

The SCU unit has two pieces of dual channel synchronous serial controllers (SAB 82525, U48 and 49) providing:

(a) one LOCAL VTP bus interface at 2 Mbit/s with advanced CMOS drivers (euro connector CN1)

(b) one CLUSTER VTP bus interface at 1024/512 Kbit/s with V11 drivers (CBUS connector CNF2)

(c) two full duplex HDLC channels at up to 64 Kbit/s, compliant with a subset of LAPB standard. Channel A is reserved in production testing phase. Channel B is used for communication with the NMS computer through an SCC interface (SCC-IF).

NOTE! ***The single-channel version of the communication controller is used instead of U49 (SAB 82526) starting from hardware version 3.0.***

2.3.2.5 A/D Converter

The SCU unit has an 8-bit CMOS A/D converter with an 8-channel multiplexer. The A/D converter is used to supervise the operating voltages of the SCU unit and the BUS1 and BUS2 voltages of the subrack

2.3.2.6 SC Interface

The SCU unit has a single asynchronous serial channel. This interface is used on service computer connection (CNF1). The baud rate of the UART U14 (82510) can be selected from 300 baud to 19.2 kbaud. The unit software sets the baud rate into 9600.

2.3.2.7 SCC Interface

On the unit there is one 2 x 10 pin header connector (CN4) for the SCC-IF X.25/V.11 interface module. The battery backup system BBS alarms can be fed into the DXX network through the alarm interface module ALARM-IF. See Fig. 10 and Fig. 11.

2.3.2.8 Cross-Connect Interface

The unit has interface to the 64 Mb/s cross-connect bus through CN5. The unit utilizes bus timing signals C16M, CLF and CLM, which are supplied by the SXU. The SXU changes data between SCU by transmitting the channel address, which again activates the data buffers in CIF ASIC. Both the received and transmitted data is transferred via their own 8-bit wide buses. The received data bus DR1 is protected by DR2.

2.3.2.9 Additional HDLC Channels (HDLC-4CH) Interface

Two 2 x 10 pin header connectors (CN2 and CN3) form the interface for the HDLC-4CH control channel expansion module.

2.3.2.10 Internal Control Buses

The SCU unit has interfaces for two internal control buses - the local VTP bus and the cluster VTP bus. The local VTP bus is used for communication between the units within one subrack and the cluster VTP bus is used for communication between the subracks of a cluster node. Both buses are synchronous serial high-speed local area networks with physically duplicated data and clock lines and interface circuits. The bit rate of the local VTP bus is 2 Mbit/s. The bit rate of the cluster VTP is 1 Mbit/s.

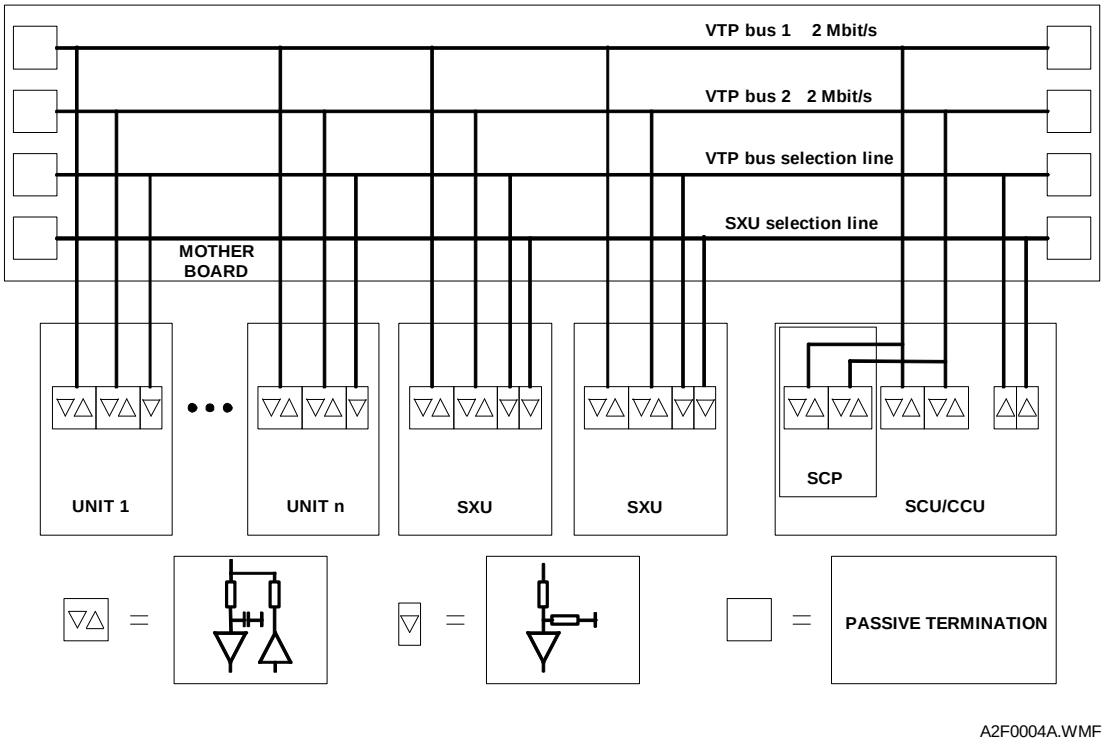


Fig. 7: Block Diagram of the Local VTP Bus

VTP is an abbreviation of the words Virtual Token Protocol which is a collision-free media access method based on the token passing principle implemented by the aid of timers. The logical link control is based on LLC3 protocol in both buses. The upper layer protocols are the same as the those of the external management interfaces of DXX nodes. The local VTP bus supports unit addresses 1…31. The cluster VTP bus supports subrack addresses 1…9. The location of the control buses of a cluster node is shown in figure below.

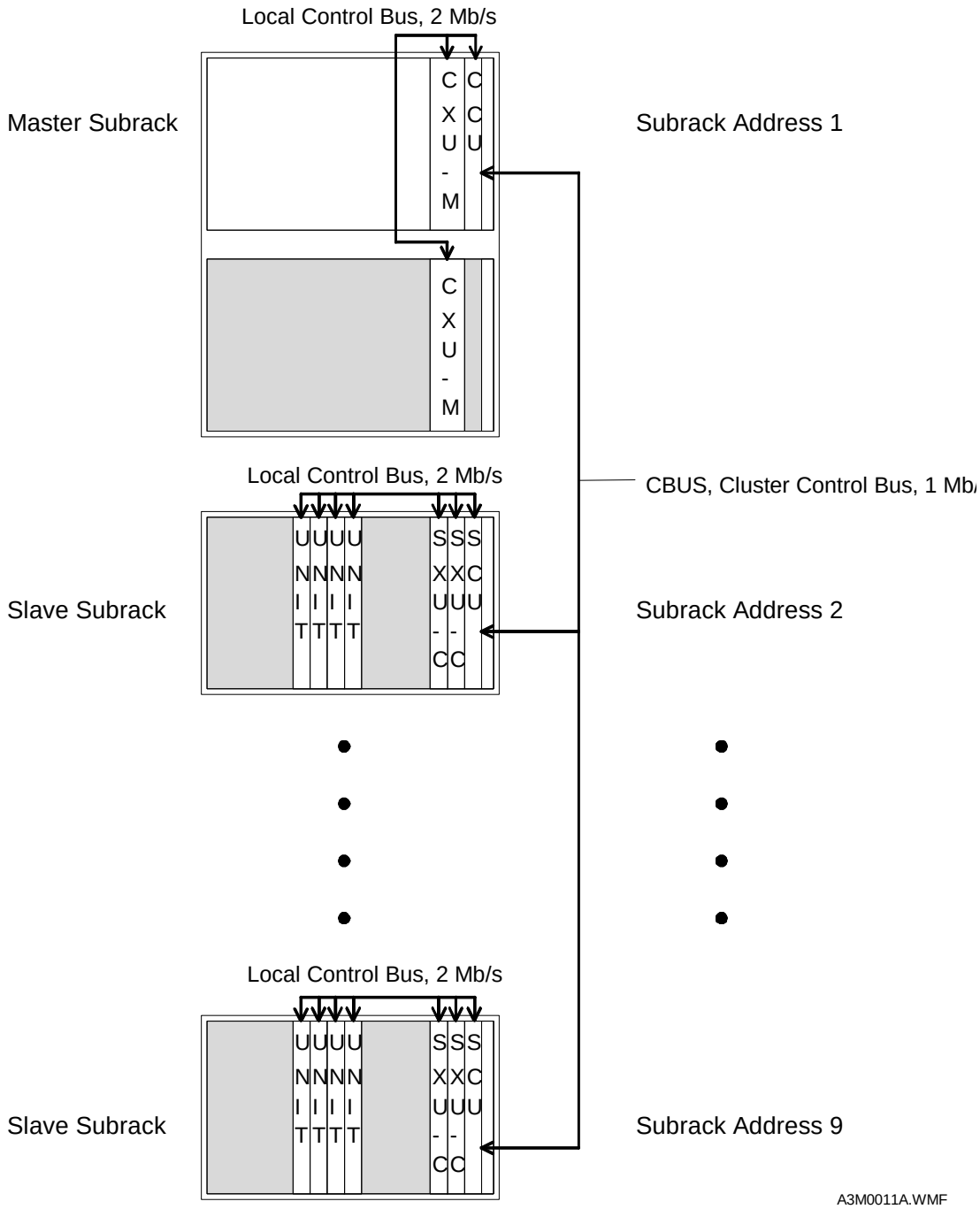


Fig. 8: Location of the Control Buses of a Cluster Node

2.3.2.11 Node Level Operations

The software of the SCU takes care of the following node-level operations:

- Node Inventory Management
- Backup of unit settings
- Protection of the cross-connect system
- Protection of control buses
- Rack alarm (PMA, DMA, MEI) control
- Event reporting to the Network Management System
- Channel test functions
- Control channel support for HDLC-4CH

Node Inventory Management

The Node Inventory Management software includes functions to get and set node and subrack identifications, to create and delete inventory, to add and remove units, to get inventory reports and to monitor the presence of registered or unregistered units. The Create Inventory operation is used to register all existing units for the inventory. The Add Unit operation is used to register a given unit for the inventory. The Delete Inventory makes all units unregistered - in other words, all units are removed from the inventory. The Remove Unit operation is used to remove a given unit from the inventory.

The Inventory Report provides the node and subrack identification data and the list of existing or registered units. The Installation Error fault condition is detected if the inventory data is not unambiguous and consistent. The Missing Unit fault condition is detected if a registered unit is not present. The Extra Unit fault condition is detected if there is an unregistered unit present in the subrack.

Backup of Unit Settings

The SCU unit stores the backup settings of all registered units for possible unit replacements. A new replacement unit will inherit the backup settings of the unit registered for the unit slot. The checking of compatibility of settings is based on the hardware types and the software types.

The backup settings are updated to the SCU unit when a unit is registered or when the settings of the unit have been changed. The backup settings are copied from the SCU unit when a registered unit is replaced by another compatible unit. The backup settings of the SCU unit itself are kept in the cross-connection unit of the subrack. The backup of cross-connection data is available only in the redundant cross-connection units if the node has a protected cross-connection system.

Protection of Cross-Connect System

The SCU unit controls the protection of the cross-connect system. The SXU type and the SXU protection option can be set. These parameters are updated automatically when the inventory is created. The inventory must be deleted before changing the SXU type, and recreated when the SXU type has been changed. The SXU protection option (protected or not protected) can be changed when there is one or no SXUs registered. In the protected system the SCU unit monitors the condition of the redundant SXUs and tries to activate one of the redundant SXUs if it has normal conditions.

The possible fault conditions for the cross-connection protection system are the following:

The Faulty Cross-Connection System fault condition is detected if there are no SXUs which can be activated, in other words, both SXUs are faulty or missing. The Forced State in SXU Activation fault condition is detected when the cross-connect protection system is not allowed to control SXU activation autonomously but is forced to keep the given state of SXU activation by a management operation.

Protection of Control Buses

The SCU unit controls the protection of the local VTP bus and the protection of the cluster VTP bus.

The local VTP bus has two alternative physical buses called Local VTP Bus1 and Local VTP Bus2 implemented by redundant interface circuits in each DXX unit and redundant set of wires on the back plane of a subrack. There is a centralized control to activate one of the alternative buses by a selection line.

The SCU unit controls the selection line in a synchronized way so that data transmission on the bus is never disturbed for the bus selection. Bus1 and Bus2 are periodically used in order to detect possible problems as soon as possible, no matter which bus will be faulty.

A checking procedure is activated when any of the units has disappeared from the inventory monitoring process. The checking procedure decides whether or not the unit is accessible by one bus only. If the unit is accessible by one bus only then the other bus must be faulty and the corresponding fault condition is detected. A test window can be used to check the local VTP status and to clear the fault condition.

The cluster VTP bus has two alternative physical buses: Cluster VTP Bus1 and Cluster VTP Bus2 implemented by redundant interface circuits in each SCU unit and redundant set of wires on the interconnection cables between the subracks of a node. There is a local control to activate one of the two receiver circuits. Data is always sent to both physical buses. The performance of physical buses is monitored and compared. When one bus is found to be worse than the other, a corresponding fault condition is detected as well.

Rack Alarm Control

The SCU unit controls the three LEDs and the corresponding relay outputs for the equipment alarms (PMA, DMA, MEI) of a subrack. The rack alarm LEDs and the corresponding relay outputs are located in the PFU or PAU units. The rack alarms, PMA, DMA, MEI, are given if any unit in the subrack has an active fault condition which requires the corresponding alarm as a consequent action. The SCU unit collects PMAs, DMAs and MEIs from the units of the subrack and sums them separately for each rack alarm.

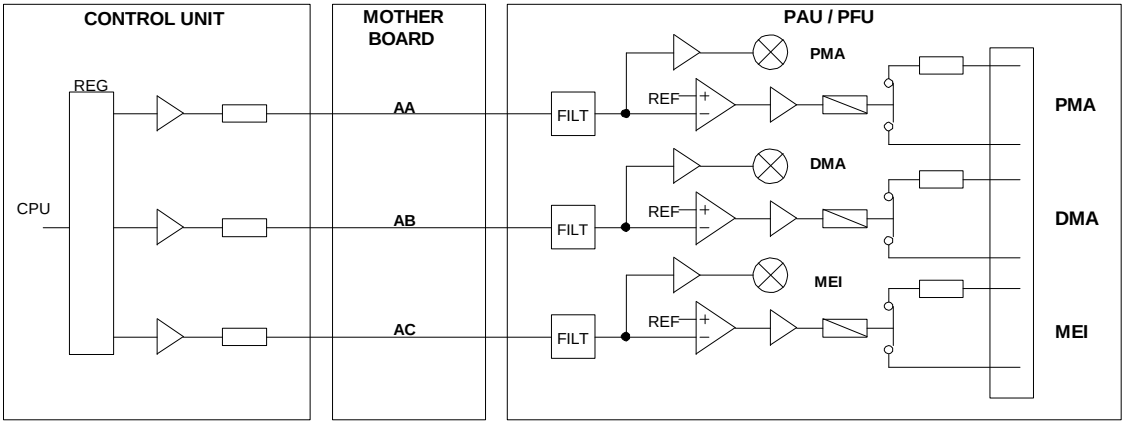


Fig. 9: Rack Alarm Control

Rack alarms can be delayed. The rack alarm delay can be set (0…600 seconds) by the user. A summed alarm must be active at least for the set delay time - not necessarily continuously - before the rack alarm is activated in PFU or PAU. The rack alarm will be passivated in PFU or PAU when the summed alarm has been continuously passive for at least the set delay time.

The rack alarm PMA and DMA can be cancelled. The rack alarm cancellation is not delayed. When PMA and DMA have been cancelled, MEI is activated as a reminder.

Event Reporting to Network Management System

The SCU unit does not only supervise the registered units of the subrack for the rack alarms but also to support subrack-level and node-level status polling from the centralized Network Management System as well. The node state report contains the status of the subracks which are not in the normal state.

The subrack state report contains the status of the units which are not in the normal state. For example, all changes in fault conditions and configuration are indicated for all units. These reports make it possible to get detailed information from the correct units for different purposes.

While the subrack state report is created, the route to the polling DXX Server is updated to the local routing table of the SCU unit from the invoke message. This route can be used to send spontaneous event reports to the DXX Server. The unit reporting modules can send event reports to the local SCU unit which then sends them to the DXX Server. The most important application is the reporting of trunk fault changes in the trunk recovery management.

Channel Test Functions

The SCU unit contains a configurable test resource which can be used for channel test functions. The test resource contains a configurable cross-connection port, test loop functions, a test pattern generator and receiver. The channel test functions include create and delete operations which are used to allocate and deallocate the test resource for a given circuit, operations to determine the test configuration, actions to activate and deactivate the test port, actions to activate and deactivate test operation and a get operation to read the test status and the test results.

The test status and the test results include the following data:

— Test status: active (true/false); running (true/false)
— Elapsed time
— Test control performance data
— Error counters
— Slip counters
— Error performance (G.821)

Control Channel Support for the HDLC-4CH

The HDLC-4CH unit is an optional module, which can be piggy-backed on a SCU unit. The HDLC-4CH unit provides four additional HDLC control channels to the DXX node and an additional backup memory for use of other units in the node.

The control channels in HDLC-4CH unit are connected to the DXX node's cross-connection bus via SCU unit which provides four cross-connection ports for the channels. The bit rates of the cross-connection ports can be configured in pairs to 0, 8, 16, 32, or 64 kbit/s. The ports can be connected through the DXX network to another node to provide transparent control channels between HDLC-4CH units. The control channels provided by the HDLC-4CH unit are used for communication between DXX nodes.

The HDLC-4CH unit's additional backup memory feature, applicable from hardware version 3.0, is used to store other unit's settings requiring large amount of memory (eg. GMU) in the same node.

2.3.3 Unit Faults

2.3.3.1 Unit Faults

Fault Condition	Status	LED	Note
Reset of Unit	PMA	R	

Power Supply Faults

Fault Condition	Status	LED	Note
VB1: + 5 V (BUS1)	PMA	R	
VB2: + 5 V (BUS2)	PMA	R	
Power + 5 V	PMA	R	
Power + 12 V	PMA	R	
Power -10 V	PMA	R	

Power Supply Faults

Fault Condition	Status	LED	Note
VB1: + 5 V (BUS1)	PMA	R	
VB2: + 5 V (BUS2)	PMA	R	
Power + 5 V	PMA	R	
Power + 12 V	PMA	R	
Power -10 V	PMA	R	

Memory Faults

Fault Condition	Status	LED	Note
RAM Fault	PMA	R	
EPROM Fault	PMA	R	
FLASH Memory Fault	PMA	R	
Missing Settings	PMA	R	
Incompatible SW in EPROM and FLASH	PMA	R	
Check Sum Error in Downloaded Pro-gram	PMA	R	

Control Bus Faults

Fault Condition	Status	LED	Note
Fault in Local VTP Bus1	DMA	Y	A test window can be used to check the Local VTP status and clear the fault.
Fault in Local VTP Bus2	DMA	Y	A test window can be used to check the Local VTP status and clear the fault.
Fault in Cluster VTP Bus1	DMA	Y	Possible in a slave subrack of a cluster node.
Fault in Cluster VTP Bus2	DMA	Y	Possible in a slave subrack of a cluster node.

Cross-Connection Protection Faults

Fault Condition	Status	LED	Note
Faulty Cross-Connection System	PMA, S	Y	Service alarm
Forced State in SXU Activation	MEI	Y	

Inventory Faults

Fault Condition	Status	LED	Note
Installation Error	PMA, S	R	Service alarm
Missing Unit	PMA, S	Y	The block number indicates the unit address. Service alarm
Extra Unit	MEI	Y	The block number indicates the unit address.

Optional External Alarms with ALARM-IF

Fault Condition	Status	LED	Note
Battery Not Ready	PMA	R	Contact closure in the external alarm input 1
AC Off	PMA	R	Contact closure in the external alarm input 2

2.3.4 Strapping Instructions for SCU

Strap S1 sets the Cluster VTP bus bit rate. Strapping on the left side (J1) means positions 2 and 3 (1024 kbit/s), and strapping on the right side means positions 1-4 (512 kbit/s).

STRAP	FUNCTION OF STRAPPING	STRAPPED 1 4	STRAPPED 2 3
S1	VTP Bit rate	512 Kbit/s	1.024Mbit/s
STRAP	FUNCTION OF STRAPPING	STRAP INSERTED	STRAP REMOVED
J1	Watchdog system	Disabled	Enabled

2.3.5 Front Panel for SCU

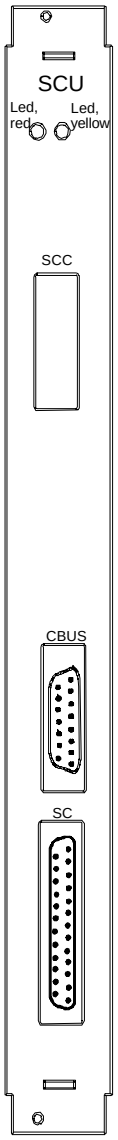


Fig. 10: SCU Front Panel (optional modules for SCC, see next page)

SCU Cluster Bus Connector (D15 Female) Pin Usage

Pin	Signal
1	Cable Shield
8	Signal Ground
6, 13	VTDT1, bidirectional
14, 7	VTCL1, bidirectional
10, 3	VTDT2, bidirectional
9, 2	VTCL2, bidirectional

SCU Local Service Computer Connector (D25 Female)

Pin	Signal
1	101 Cable Shield
2	103 transmitted data
3	104 received data
4	105 request to send
5	106 ready for sending
6	107 data set ready
7	102 signal ground
8	109 signal detector
20	108 data terminal ready
9…19	no connection
21…25	no connection

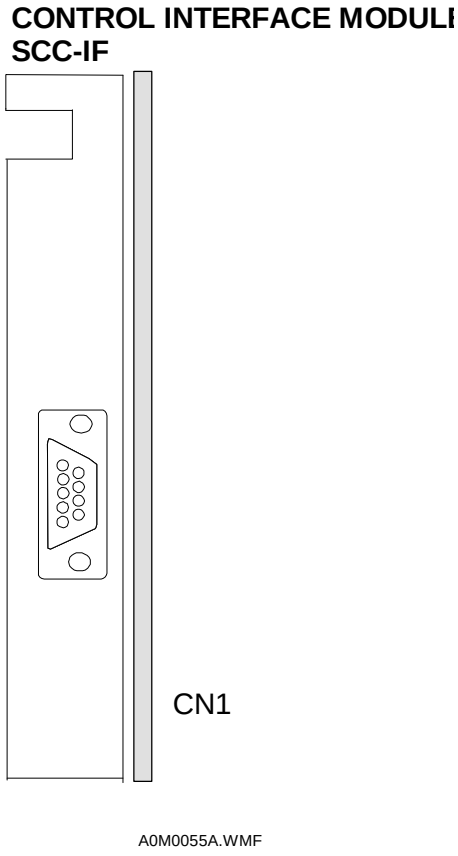


Fig. 11: Control Interface module SCC-IF

SCC-IF NMS Computer connector V.11 levels (D15 male)

Pin	Signal
1	Cable shield
2, 9	T(A), T(B), output
3, 10	C(A), C(B), output
4, 11	R(A), R(B), input
5, 12	I(A), I(B), input
6, 13	S(A), S(B), input/output
8	G, signal ground
7, 14, 15	no connection

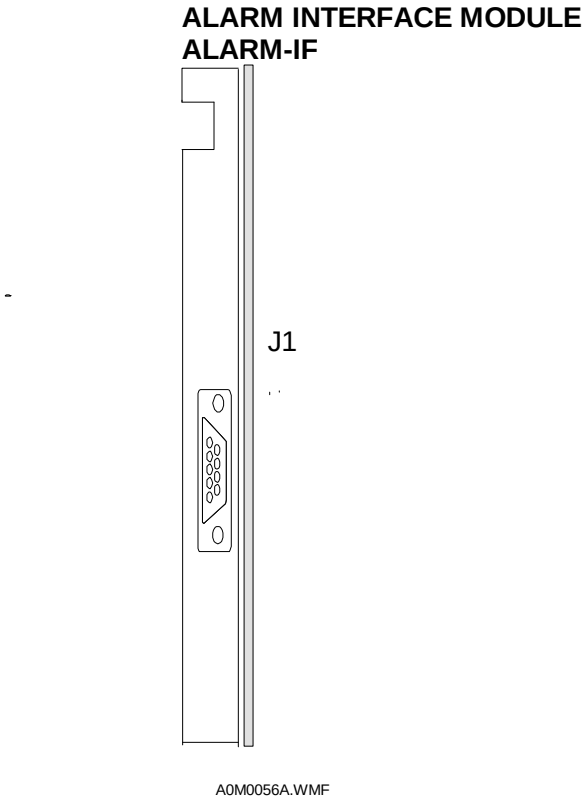


Fig. 12: Alarm Interface module Alarm-IF

Alarm Interface module pin usage (D9 female connector)

Pin	Signal
1	Contact alarm 1, input
2	No connection
3	Contact alarm 2, input
4	No connection
5	No connection
6	Return 1, signal ground
7	No connection
8	Return 2, signal ground
9	No connection

2.3.6 Cabling for SCU/CCU

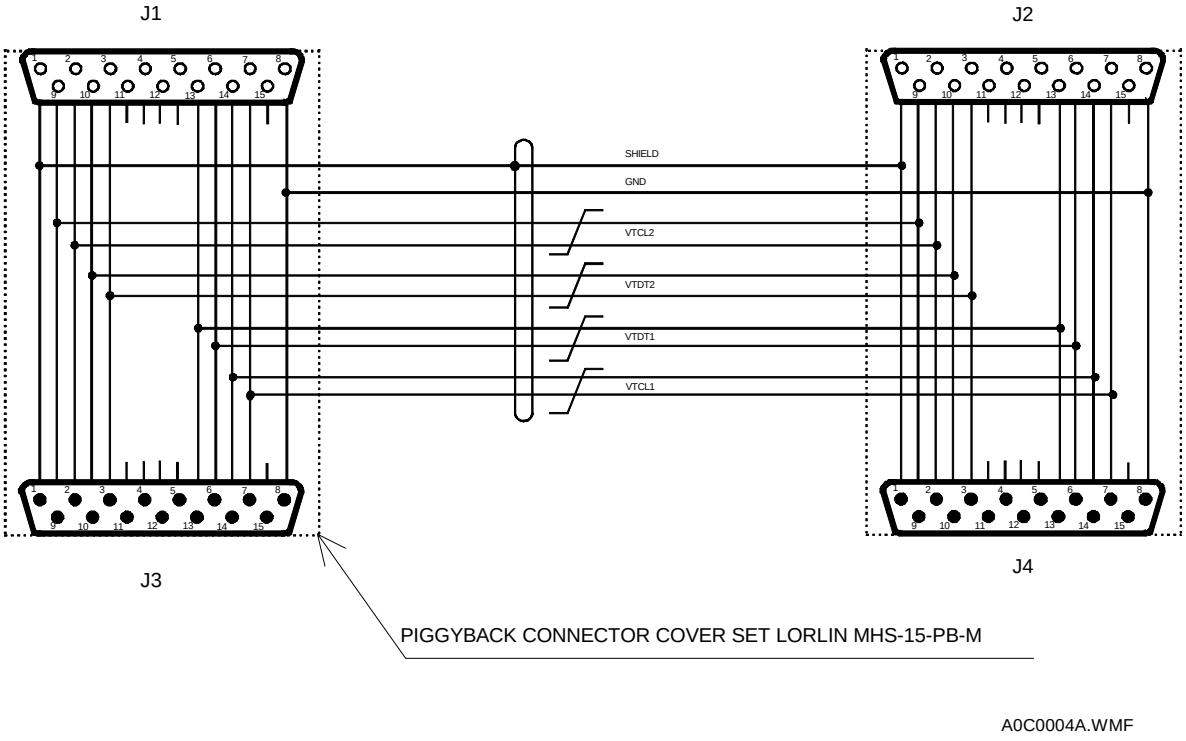


Fig. 13: SCU/CCU Control Bus Cable

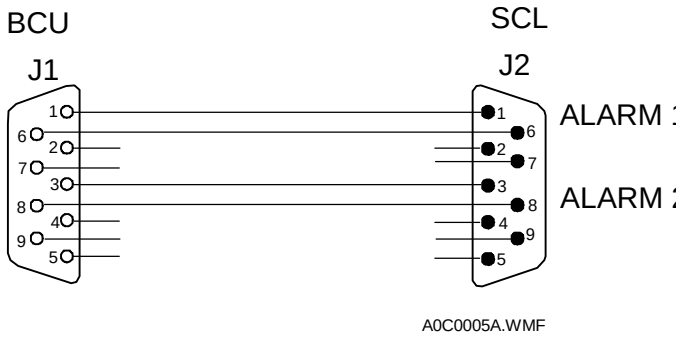


Fig. 14: BCU-SCL ALARM Interface cable

NOTE! ***Pins 6 and 8 of the connector J1 can be earthed in BCU unit if necessary.***

The same cable can also be used with the PFU-B or PFU-A.

2.3.7 Control Interface Technical Specifications

SC Interface

Purpose	Management interface for SC/NMS
Electrical interface	V.28
Data bit rate	9600 b/s asynchronous
Character format	8 bit, no parity, 1 stop bit
Connector type	ISO 2110, D-type 25-pin female connector
Interface signals	101,102,103,104,105,106,107,108 and 109
Protocol	Layers 2…7 proprietary

SCC Interface

Purpose	Management interface for NMS
Electrical interface	V.11/X.27
Data bit rate	64 kb/s synchronous
Frame formats	F, A, C, FCS, F or F, A, C, Info, FCS, F (basic operation)
Connector type	ISO 4903, D-type 15-pin male connector
Interface signals	G, T, R, C, I, S
Protocol	LAPB + X.25 PLP + Layers 3…7 proprietary

CBUS Interface

Purpose	Cluster Control Bus
Electrical levels	V.11, redundant drivers and receivers
Data bit rate	1024 kbit/s synchronous
Connector type	ISO 4903, D-type 15-pin female connector
Interface signals	VTDT1, VTDT2 and VTCL1, VTCL2
Protocol	Layers 2…7 proprietary
Physical length of the bus	20 m, maximum

2.4 SXU Cross-Connect Unit

2.4.1 General

The cross-connect unit SXU has three variants. In a Basic Node either SXU-A or SXU-B is employed. SXU-C is used in a Cluster Node's slave subrack. All SXU variations have a strictly non-blocking time-space matrix for 64 kbit/s signals.

SXU-A cross-connects n x 64 kbit/s XB-channels with possible signalling (XD-channels) as well as a limited number of n x 8 kbit/s XB-channels. SXU-A is intended mainly for network access nodes.

SXU-B is intended for network transit nodes requiring extensive use of n x 8 kbit/s connections. SXU-B covers the functions of the SXU-A providing also n x 64 kbit/s- and XD-channel connection.

SXU-C provides n x 64 kbit/s plus XD-channel connection in a Cluster Node.

2.4.2 SXU Operation

2.4.2.1 Subrack Cross-Connect Bus (X-Bus) Structure

The cross-connect bus covers unit positions 2 to 16 (17) in the subrack back plane. Position 17 is reserved for an optional bus extension card to the lower shelf in a double-shelf subrack.

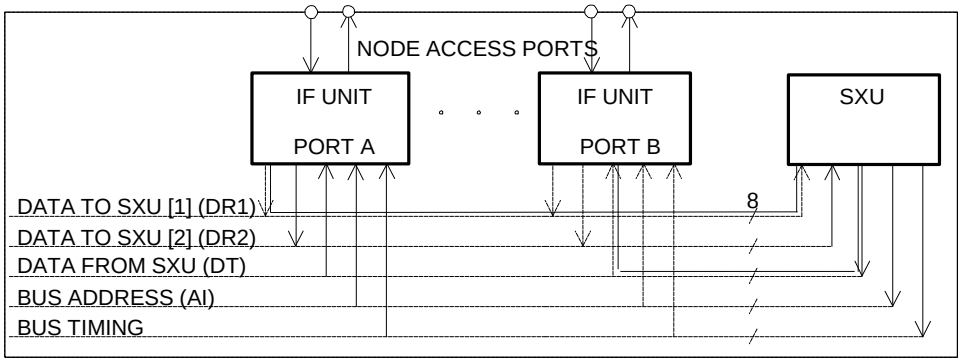
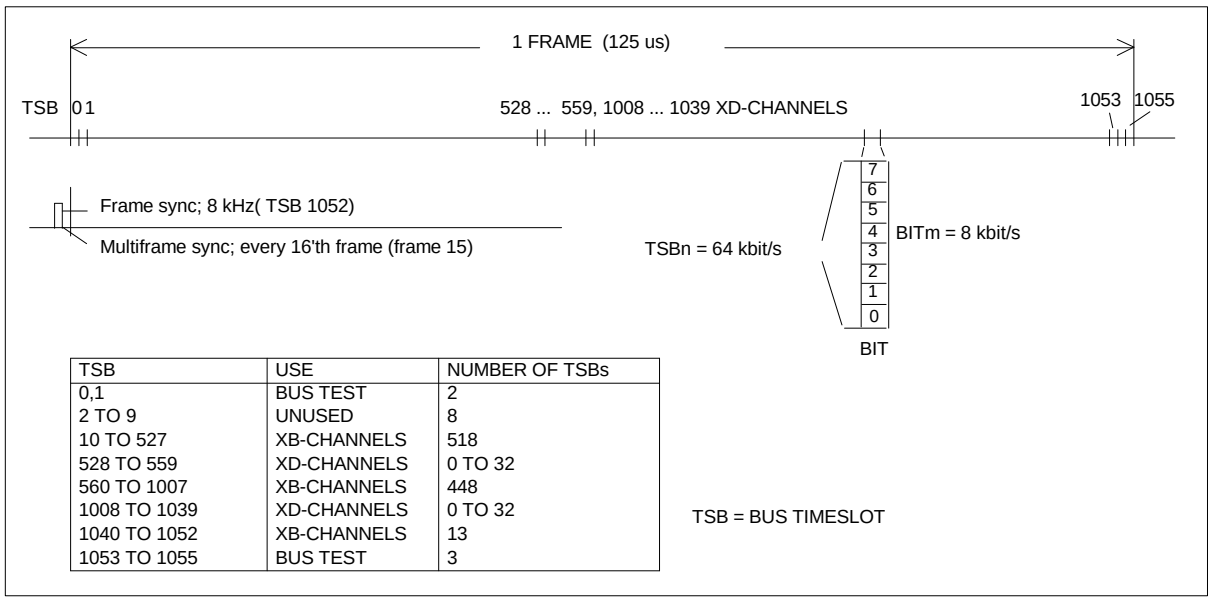


Fig. 15: X-Bus Signals

The X-bus operates synchronously. Interface units (IF-units) adjust mesochronous or plesiochronous access port signals into the X-bus by bit buffering. IF-units with a frame structure also buffer the frame (multiframe) phases.

SXU supplies the bus clock (16896 kHz), frame timing (8 kHz) and multiframe timing (0.5 kHz). SXU generates a port address for each cross-connected bus time slot. A port exchanges a data byte with SXU when the port recognizes its address. Ports with a frame structure receive the frame time slot number explicitly. The data bus in the direction from the IF-units to SXU is doubled for redundancy.



TSB	USE	NUMBER OF TSBs
0,1	BUS TEST	2
2 TO 9	UNUSED	8
10 TO 527	XB-CHANNELS	518
528 TO 559	XD-CHANNELS	0 TO 32
560 TO 1007	XB-CHANNELS	448
1008 TO 1039	XD-CHANNELS	0 TO 32
1040 TO 1052	XB-CHANNELS	13
1053 TO 1055	BUS TEST	3

Fig. 16: Logical Structure of the X-Bus

The X-bus frame is divided into 1056 bus time slots (tsB) numbered from 0 to 1055. Each tsB has a capacity of 64 kbit/s. Each of the eight bits in a tsB can be considered as a separate 8 kbit/s channel. For XD-channel cross-connection up to 32 (in SXU-A) or 64 (in SXU-B) tsBs can be further multiplexed by the 16 frames long multiframe. The XD-time slots are cross-connected bit-by-bit creating n x 0.5 kbit/s channels.

Five time slots are reserved for node monitoring. The remaining 1051 bus time slots are reserved for cross-connection of user data.

2.4.2.2 X-Bus Allocation

X-bus capacity is allocated by the SXU software based on selected port parameters. Ports are classified as even and uneven ports.

Even Ports

2048 and 8448 kbit/s ports on the GMH-unit can get an even allocation providing minimum signal delay. The operator creates an even allocation by choosing a 2 frame receive buffer. A longer buffer results in an uneven allocation.

When the operator locks the parameters of an even port, bus capacity is allocated according to the port's signal rate. This capacity can be released only by unlocking the port.

The X-bus is divided into eight 8448 kbit/s even groups consisting of regularly every eighth bus time slot (TSB). A 8448 kbit/s group can be further divided into four 2048 kbit/s even groups. These groups have fixed bus time slots. A maximum of 32 even 2048 kbit/s ports can be locked in one subrack.

Uneven Ports

Other than 2048 and 8448 kbit/s ports get an uneven allocation. Also 2048 and 8448 kbit/s ports get an uneven allocation if receive buffer is longer than 2 frames. An uneven port does not reserve tsBs for XB-channels until the time slots are cross-connected. A possible XD-time slot is reserved when the port is locked. More than 32 uneven 2048 kbit/s ports can be accommodated in a node, if part of the time slots are not cross-connected and if the signalling capacity is not limiting.

2.4.2.3 An Example of the Signal Cross-Connection Procedure

64 kbit/s XB-Signal Connection

The following sequence details the procedure when SXU cross-connects a byte between two 64 kbit/s ports. shows the data path in the direction from port A to port B (dashed line).

When the operator locks the port parameters the port is automatically allocated one tsB. The operator creates a cross-connection between the two ports.

In each bus frame for ports A and B:

— SXU outputs the port's address on the address bus
— SXU reads a cross-connect address from an address memory and using the address reads a data byte from the data memory
— The port and the SXU exchange a data byte
— SXU writes the byte it received into a data memory
— The port sends the byte it received to the access interface. The delay of XB-channels in the SXU is one frame (125 µs). The total delay through a node also includes the buffer delays in the IF-units.

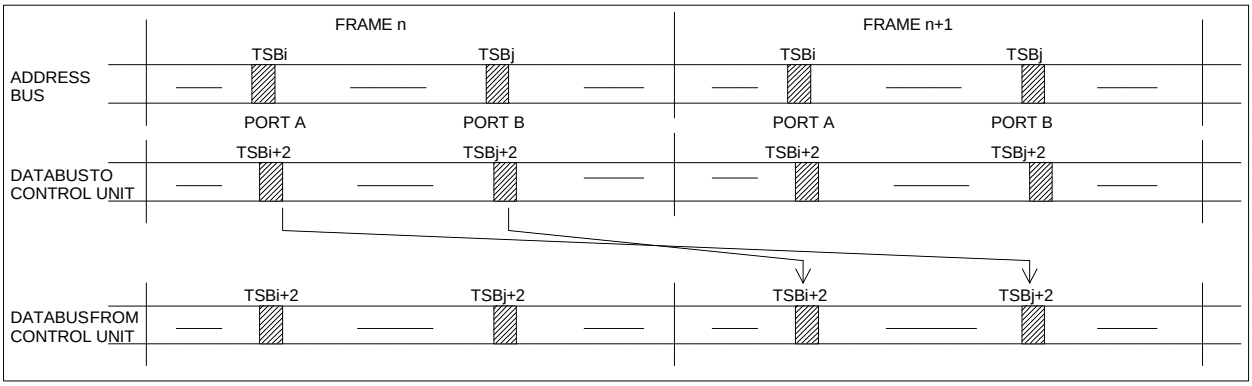


Fig. 17: Data Byte Exchange on the X-Bus

8 kbit/s XB-Signal Connection

The data exchange on the X-bus is similar to that of the 64 kbit/s signal. A whole byte is always transferred. SXU assembles the byte bit-by-bit during eight consecutive time slots. Bits, which have not been cross-connected, are set to idle state '1'. Signal delay is one frame within the SXU.

0.5 kbit/s XD-Signal Connection

The procedure is similar to the 8 kbit/s connection, but here the multiframe structure is employed. The delay in the SXU is one multiframe (2 ms).

2.4.2.4 Node Clock System

The main oscillator (PLL1) runs at a frequency of 16896 kHz. Accuracy in internal timing mode is ±30 ppm over the operating temperature range. For jitter and wander specifications, see Technical Specifications. The main oscillator can be locked to an external source or to the received clock of an access interface. Two synchronization buses are provided for transferring clocks to the SXU.

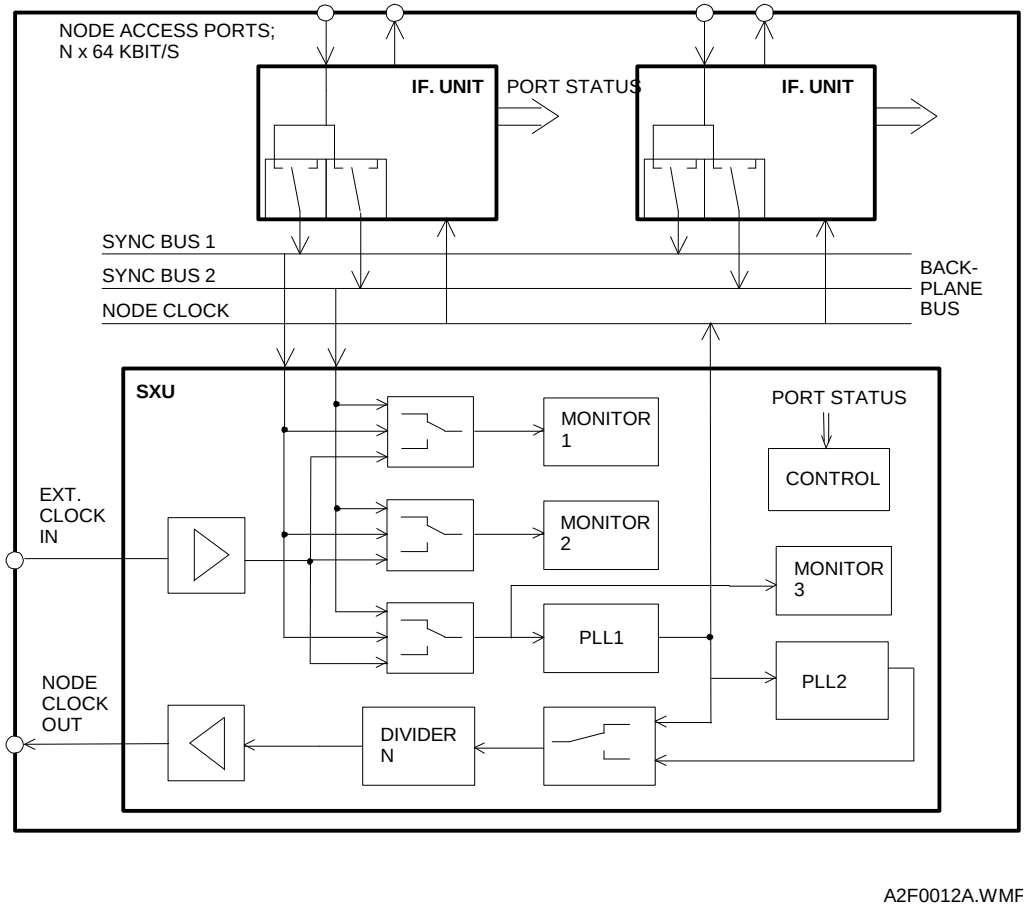


Fig. 18: Node Clock System

Auxiliary Oscillator

An auxiliary oscillator (PLL2) is locked to the PLL1 providing frequencies in the 2048 kbit/s hierarchy for the clock output interface. Frequency of oscillation is 8192 kHz. PLL2 also supplies the 2048 kHz clock used for connection to the subrack control bus.

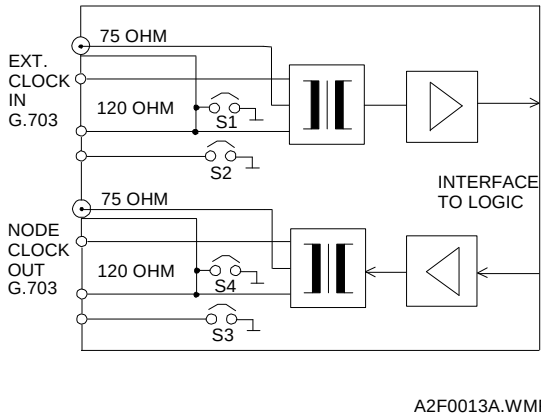


Fig. 19: Clock Interfaces

Clock Interfaces

An input interface for an external clock and an output interface for the node clock are provided. The interfaces comply with the ITU-T rec. G.703 § 10. Connectors are located in the SXU front panel. For interface specifications see Technical Specifications.

The quality level (QL) of clock signal

Each synchronization source (external clock interface or trunk line) has a parameter called Quality level and it has been defined as numerical values from 1 to 7 where 1 is the highest and 6 the lowest one (7 means ‘don’t use this clock’; used to prevent timing loops). The quality level of external clock is parameterizable for each node separately through NMS Master Clock window. (Usually value 1 is used.) The quality level of a clock obtained from trunk line is determined in the node where the clock originates. (In PDH network, it is usually 1 if the original source is an external clock and 6 if the original source should be the internal clock of some node.) If a node should lose other clock sources and fall to internal clock, the quality level value is the one parametrized for internal clock in NMS Master Clock window (usually value 6 is used).

For PDH trunks such as GMH, the quality level is transmitted over the network via Neighbor Node Monitoring messages. For SDH trunks such as GMU, there is a mapping between the SSM (Synchronization Status Message) quality levels.used in SDH networks and the proprietary Ericsson DXX quality levels, as follows.

SDH quality level	Interpretation in Ericsson DXX
QL-PRC	1
QL-SSU-T	2
QL-SSU-L	4
QL-SEC	5
QL-DNU	7

Ericsson DXX quality level	Interpretation for SDH
1	QL-PRC
2	QL-SSU-T
3	QL-SSU-L
4	QL-SSU-L
5	QL-SEC
6	QL-SEC
7	QL-DNU

Quality levels can be disabled through NMS Master Clock window, which means that the quality levels are ignored when selecting the node clock.

Quality Level Message Delays in Basic Node

The distribution method of the quality level of a clock is different for SDH and PDH parts of the network, and so are the distribution delays.

In SDH trunks (for example, STM-1 interfaces in GMU units) the quality level is continuously transmitted in SSM messages in the SOH bytes of an STM-1 (ITU-T Recommendation G.707). The cross-connection unit, which controls the clock, exchanges the SSM messages through the cross-connection bus, which is a fast method. Consequently, the delay for passing an SSM message on to another node is short and depends mostly on data processing delay in the cross-connection unit. For SDH trunks, it less than 450 ms.

In PDH trunks (such as trunks between GMH units), the quality level is repeatedly sent to the far end using neighbour node messages (NNM). The interval between two NNM messages may depend on the trunk unit type, but it is typically 1 s. The cross-connection unit polls each trunk unit frequently, sends the current quality level, and receives the incoming quality levels. The delay between two polls of a single unit depends on the node type (cluster or basic).

Consequently, the delay for passing a quality level message on to another node through PDH trunks is the sum of three values: the polling delay for the incoming trunk unit, the polling delay for the outgoing trunk unit, and the delay in the NNM process of a trunk unit. All three delays are random, and their maximum values are as follows:

1. Polling delay for PDH units: max 4 s in basic nodes.
2. NNM process delay for PDH trunks: max 1 s.

Average values can be estimated by dividing these three values by two. For example, the average delay between two GMH trunks in a basic node might be 2.0 + 2.0 + 0.5 s = 4.5 s.

Fallback List

In a DXX network 2 Mbit/s and 8 Mbit/s trunk lines and the SXU's external clock interface are normally used to transfer timing to the node. While the node clock can be synchronized from interfaces at lower rates (n x 64 kbit/s), it should be noted that synchronization from 2 Mbit/s and 8 Mbit/s signals results in better controlled wander properties.

The operator selects in the Master Clock-menu of the Node-window ports for the fallback list and assigns their priority. Up to five ports can be entered.

Among the clocks in the fallback list, the clock signal which has the highest quality level and the status of which is OK, is the one to which the master clock is synchronized. If clock signals have the same QL, the clock to which the master clock is synchronized is the one with the highest priority according to the Fallback list. However, if quality levels are disabled (see the previous section), all clocks are considered to have the same quality level. If no clock in fallback list is usable, the node uses the internal clock of SXU.

Clock Monitoring and Alarms

The SXU monitors the clock selected and also the next choice on the fallback list. The external clock is monitored when enabled.

Fallback list clocks are also monitored by the interface units. By a major fault in a port's rx-signal, the IF-unit clamps the clock (on SYNC BUS 1/2) and sends a clock status message to the SXU. SXU's monitoring circuit opens the phase-locked-loop maintaining the clock frequency until the processor selects another clock. Internal timing is selected if all clocks on the fallback list have failed.

2 Mbit/s and 8 Mbit/s interfaces with a frame structure can employ a dedicated bit in the frame as a clock far end alarm bit (FEA). It is used on trunks transferring timing between nodes. If an intermediate node in a network loses its synchronization, the alarm bit is transmitted from all its interfaces. The receiving node's IF-unit then clamps the clock on sync bus 1/2.

After a fault is cleared the IF-unit gradually clears the clock status. The operator can enter a clock acceptance time in the Master Clock-menu. A clock is not selected again until its status has been good over the acceptance time.

The SXU supervises that the PLL1 is locked to the clock source. A phase-locked-loop alarm is generated if the source frequency is out of range or if it contains jitter more than specified in Technical Specifications.

Clock Output Interface

Node clock output is provided at the external interface in the SXU. The output is activated and its frequency selected from the Master clock window. The output control function, when set to on state, disables the output when the SXU is in internal timing or locked to the external interface. When output control is off, clock output is active regardless of the fallback list state.

Clock Faults Monitored in the SXU (software version 6.5 or earlier)

Fault description	Status	Led	Alarm message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock enabled and missing	PMA	Red	Loss of external clock
External clock on fallback list, clock interface disabled	MEI	-	External clock warning
Locking to a clock failed: input frequency out of tolerance range (typically external clock)	PMA	Red	Phase-locked-loop alarm
Clock far end alarm (individual for each link)	MEI	Yel	Clock far end alarm

NOTE!

In protected SXU nodes, faults which light red LED cause protection switch to the redundant SXU (unless the redundant SXU has the same problem).

Clock Faults Monitored in the SXU (software versions 6.6 to 6.8)

Fault description	Status	Led	Alarm message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock enabled and missing	PMA	Yel	Loss of external clock
External clock on fallback list, clock interface disabled	MEI	-	External clock warning
Locking to a clock failed: input frequency out of tolerance range (typically external clock)	PMA	Yel	Phase-locked-loop alarm
Clock far end alarm (individual for each link)	MEI	Yel	Clock far end alarm
Faulty clock source (individual for each link); see description below	MEI	Yel	Faulty clock source
SSM clock quality parameter from an SDH interface in unstable	MEI	Yel	Unstable SSM

NOTE!

In protected SXU nodes, none of these faults causes protection switch. In particular, if the active SXU loses external clock but the redundant SXU does not, the node cannot utilize the external clock at all.

Clock Faults Monitored in the SXU (software version 6.9 and later)

Fault description	Status	Led	Alarm message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock enabled and missing	PMA	Yel	Loss of external clock
External clock on fallback list, clock interface disabled	MEI	-	External clock warning
Locking to a clock failed: input frequency out of tolerance range (typically external clock)	PMA	Yel	Phase-locked-loop alarm
Clock far end alarm (individual for each link)	MEI	Yel	Clock far end alarm
Faulty clock source (individual for each link); see description below	MEI	Yel	Faulty clock source
SSM clock quality parameter from an SDH interface in unstable	MEI	Yel	Unstable SSM
External clock on fallback list but missing, and no other OK clock available	PMA	Red	Clock failure switchover

NOTE! ***In protected SXU nodes, faults which light red LED cause protection switch to the redundant SXU (unless the redundant SXU has the same problem).***

If the node clock supplied by the SXU should fail, the GMH/GCH-A units transmit an independent clock with a basic frequency tolerance to output ports. Node clock alarm is generated by the IF-units.

Clock Faults Monitored in the SXU (software version 10.1 and later)

Fault description	Status	Led	Alarm message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock enabled and missing	PMA	Yel	Loss of external clock
External clock on fallback list, clock interface disabled	MEI	-	External clock warning
Locking to a clock failed: input frequency out of tolerance range (typically external clock)	PMA	Yel	Phase-locked-loop alarm
Faulty clock source (individual for each link); see description below	MEI	Yel	Faulty clock source
SSM clock quality parameter from an SDH interface in unstable	MEI	Yel	Unstable SSM
External clock on fallback list but missing, and no other OK clock available	PMA	Red	Clock failure switchover
Indicates used clock position in fallback list (individual for each list entry 2-5)	MEI	Yel	Fallback List Entry N Used

If the node clock supplied by the SXU should fail, the GMH/GCH-A units transmit an independent clock with a basic frequency tolerance to output ports. Node clock alarm is generated by the IF-units.

Faulty Clock Source Alarm

In software versions 6.6 and later, the following handling of phase-locked-loop problems is implemented.

Typically the actual problem is that the frequency of external clock input of the node is distorted so much as to exceed the tolerance of the phase-locked loop controlling the master clock. If such a problem is persistent, the clock source is marked as faulty, and the 'faulty clock source' alarm for that entry in the fallback list is raised. A clock which is marked as faulty cannot be used as the master clock of the node. When the network operation has fixed the original problem, it is necessary to reset the 'faulty clock source' alarm through NMS. This is done by updating the fallback list thorough NMS Master Clock window.

As the faulty clock source alarm prohibits further use of the clock without human intervention, it is implemented so that the alarm is not raised if the problem appears to be only temporary. The following figure describes how the alarm is raised. There is a counter (cnt) which is zero if the clock has not had phase-locked loop problems recently and increases if problems appear. If the counter grows too high, the alarm is raised.

Note that in States 1 and 2 the clock is considered usable, and in States 3 and 4, unusable.

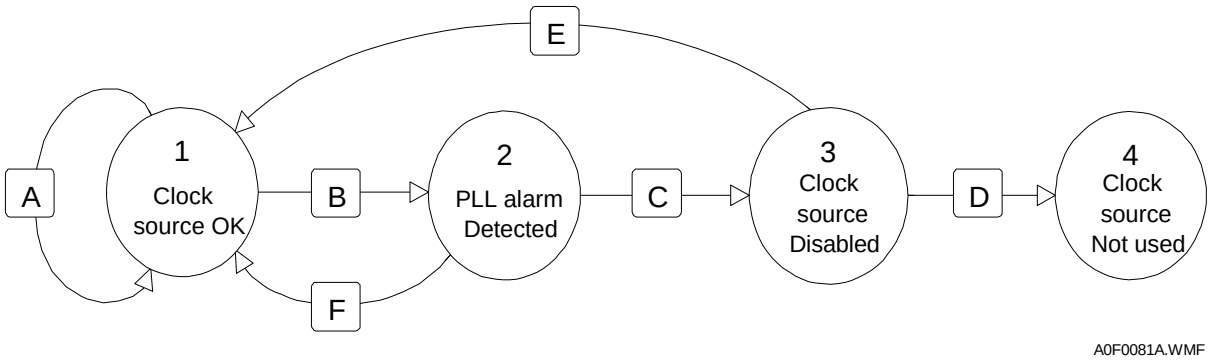


Fig. 20: Clock source

A - If cnt > 0 and no faults has occured for 5 minutes cnt is decremented by 1
B - PLL alarm occurs and cnt is incremented by one
C - PLL alarm on for more than 10 s
D - If cnt > 2 clock source is disabled permanently after 60 s (Until it is enabled from NMS)
E - If cnt < 3 clock source is enabled again after 60 s.
F - No PLL alarm during 10 s

2.4.2.5 Clear Channel Support in SXU

Unit software version 10.1 and later for SXU supports dynamic clear channel switching used for EPS (Voice/FAX compression) units. EPS does not support high speed modems, in particular V.32 and V.34 (see EPS release notes). If EPS compressed voice band circuits are used in applications where these modems are used, the modem calls will fail. To allow general use of compressed voice band channels (i.e., all common voice band traffic is supported) a dynamic 64kbps clear channel is provided when data modems are in use.

Configuration has two end nodes with EPS units capable of clear channel support. Nodes can be protected or unprotected. SXU will communicate to peer EPS Unit(s) and far SXU with messages using paths defined in parameters. Intermediate nodes do not have any requirements for SXU unit software version. The clear channel parameters are maintained with NMS and they are only stored to flash lists in SXU. This means that in an unprotected node there are no backups in the node. In a protected node the parameters are protected in the same way than other cross connection information. If the list system in the passive SXU unit is not compatible with the active SXU it is indicated by a fault (Passive Flash Version Fault) in the active SXU.

Clear Channel Concepts

Clear Channel Group (CCG):
A CCG is the administrative unit within which clear channel switching takes place. It includes a set of compressed and clear channel circuits between two end nodes, and some additional information related to the switching operation (communication path, statistics, etc.). The compressed portion of a compressed circuit in a CCG may be bypassed by rerouting (switching) the circuit to a clear channel circuit in the same CCG. To avoid configuration and allocation conflicts between the two end nodes, one of the nodes is designated Master and the other Slave for the CCG. Maximum number of CCGs in SXU is 15.

Compressed Circuits (CMC):
Compressed circuits are configured as usual. Maximum number of CMCs in SXU is 108.

Clear Channel Circuits (CLC):
These are 64kbps circuits configured in advance between the end nodes of compressed circuits. These use a new NMS circuit type: Shared Segment. Maximum number of CLCs in SXU is 27.

Control Channel (CNC):
A control channel between SCPs in the end nodes is configured to ensure fast exchange of switching protocol messages. The SCP HDLC ports are configured as SUAP (rather than General bound to HDLC trunk, as used for NMS control channels) and a circuit is routed between them using NMS circuit type Control Channel. Each SXU is informed of the control path by the NMS.

Switching to Clear Channel

When a Clear Channel Group is activated, active compressed circuits (CMCs) are able to request a clear channel from the SXU when a modem call is detected. The compressed circuit is switched to a clear channel in a manner designed to avoid disrupting the modem negotiation process. The clear channel is used for the duration of the modem call and released when the modem call ends.

Clear Channel Faults Monitored in SXU

Fault description	Status	Led	Alarm message
SXU cannot communicate with the peer SXU in the far end node of CCG	PMA	Yel	CCG communication fault
Compressed Channel unusable for switching, xc fault	MEI	-	CCG CMC fault (DELTA)
The number of free CLCs have decreased below threshold at least once during the current 15 min period (see CCG Alarm threshold attribute)	MEI	-	CCG threshold alarm (DELTA)
Switch to CLC is blocked at least once during the current 15 min period	MEI	-	CCG blocking alarm (DELTA)
Switch to CLC failed to complete at least once during the current 15 min period	MEI	-	CCG switch request failed (DELTA)

Clear Channel Statistics in SXU

The statistics are counted for periods of 15 minutes and for periods of 24 hours. Statistics are kept for the current period and the previous period.

— Number of clear channels active in group at beginning of period
— Maximum number of clear channels in use
— Minimum number of clear channels in use
— Number of calls incoming (switch requests where this end is called end)
— Number of calls outgoing (switch requests where this end is calling end)
— Number of calls released (ended) during period
— Total duration of calls that ended during the period (seconds)
— Number of switch requests blocked (failed because no clear channels available)
— Number of switches failed (did not complete due to protocol error or other failure)
— All time maximum number of clear channels in use (not by period)

2.4.3 SXU Fault Monitoring

2.4.3.1 SXU Internal Operation Monitoring

The internal data busses of the SXU are continuously monitored by looping a test byte within the SXU. The unit processor's data memory, program memory and non-volatile memory are constantly monitored.

SXU monitors the cross-connect address and port address memories when cross-connections are made.

Memory Faults Monitored in the SXU

Fault description	Status	Led	Alarm message
X-connect memory fault	PMA+S	Red	X-connect RAM fault
X-connect matrix error	MEI	-	ASIC latch warning
X-connect matrix fault	PMA+S	Red	ASIC latch error
SXU internal cross-connect fault	PMA+S	Red	X-connect loop error
Processor memory fault	PMA+S	Red	RAM fault
Processor program memory fault	PMA+S	Red	EPROM fault
Processor non-volatile memory fault	PMA+S	Red	FLASH error

Subrack Monitoring

The SXU runs a continuous test in time slot 1053, in which each active port loops back a test byte sent by the SXU (two complementary patterns used). If all ports fail, an 'X-bus 1/2 fault' is given and the redundant data bus is switched on. If the address or the timing bus fails, which can not be excluded by a bus switching, an 'X-connect bus fault' is generated.

X-Bus Faults Monitored in the SXU

Fault description	Status	Led	Alarm message
Port failure	PMA+S	Yel	Unit n IA fault
X-bus 1/2 fault	DMA	Yel	X-connect bus 1/2 fault
X-bus fault	PMA+S	Red	X-connect bus fault

Power Supply Monitoring

The SXU contains an analogue-to-digital converter for supervising the unit power supply voltage. A reference voltage is provided in the SXU.

Power Supply Faults Monitored in the SXU

Fault description	Status	Led	Alarm message
Unit supply voltage + 5/+12/-10 V out of range	PMA+S	Red	Power + 5/+12/-10 V

SXU Protection

The SXU can be doubled for redundancy. The active SXU is indicated by a green led. The stand-by unit receives same control and cross-connection messages as the active unit and adjusts to the X-bus timing.

The SCU controls the switching of the SXUs based on response to polls and on alarm status. A red alarm in results in a switch over. SCU enables one SXU and disables the other SXU with hardwired signals via the back plane. The time from a fault detection to the switch over is short. In protected operation a PMA alarm from the stand-by SXU is transformed into a MEI-alarm.

In the SXU software version 10.1 and later there are extended lists in the flash that are not supported by older SXU versions (clear channel support). The new SXU is able to indicate this incompatibility with the following fault.

Incompatibility Faults Monitored in the New SXU 10.1

Fault description	Status	Led	Alarm message
Passive SXU needs software upgrade (or is missing)	MEI	-	Passive Flash Version Fault

2.4.4 SXU Strapping Instructions

All SXU variants have identical straps. Select either the coaxial (75 Ω) or the symmetrical (120 Ω) clock interface (if neither is used, the straps are irrelevant).

The ITU-T rec. G. 703 § 10 recommends that the output cable shield is grounded and that the input shield can be grounded. Additionally the possibility to disconnect the output from ground is provided (not recommended for EMC reasons).

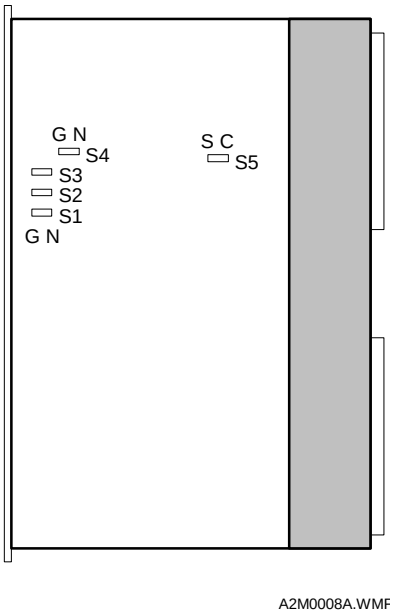


Fig. 21: Location of straps on SXU

SXU Strapping when Coaxial Interface Used

Strap	Pos.	Description
S1	N	Input coaxial cable shield not grounded
	G	Input coaxial cable shield grounded
S2	*	Don't care
S3	*	Don't care
S4	N	Output coaxial cable shield not grounded
	G	Output coaxial cable shield grounded
S5	C	Always (information of the position to the software)

SXU Strapping Symmetrical Interface Used

Strap	Pos.	Description
S1	N	Always
S2	N	Input symmetrical cable shield not grounded
	G	Input symmetrical cable shield grounded
S3	N	Output symmetrical cable shield not grounded
	G	Output symmetrical cable shield grounded
S4	N	Always
S5	S	Always (information of the position to the software)

2.4.5 SXU Technical Specifications

Impedance	75 Ω coaxial or 120 Ω symmetrical (connect one at a time)
Nominal frequency	N x 64 kHz; N = 1…132
Frequency tolerance	± 50 ppm
Connector	SMB-connector male or 9-pin D-connector female
Input attenuation	6 dB at 2048 kHz max. relative to the output pulse
Input jitter tolerance	see "Node Clock Jitter and Wander" on page 42
Return loss	15 dB min. at 2048 kHz
Over voltage protection	G.703 ANNEX B with an amplitude of 50 V
Continuous signal level	5 V rms max.
Grounding	cable outer conductor can be grounded

Impedance	75 ohms coaxial or 120 ohms symmetrical (one load at a time)
Connector	SMB-connector male or 9-pin D-connector female
Output pulse at 2048 kHz	see (G.703 § 10.2)
Pulse amplitude	V min = 0.75 V, V max. = 1.5 V at 75 ohms V min = 1.0 V, V max. = 1.9 V at 120 ohms
Nominal frequency	8448, 2048, 1024, 512, 256, 128, 64 kHz
Output jitter	(see Node Clock Jitter and Wander below)
Over voltage protection	G.703 ANNEX B with an amplitude of 50 V
Grounding	cable outer conductor can be grounded

Node Clock Jitter and Wander

2/8 Mbit/s and clock port output, internal timing	0.05 UIp-p max.
2/8 Mbit/s port output, node synchronized from an external clock at 2048 kHz containing no jitter	0.05 UIp-p max.
2 Mbit/s port output, node synchronized from an interface at 2 Mbit/s containing no jitter	0.10 UIp-p max.
8 Mbit/s port output, node synchronized from an interface at 8 Mbit/s containing no jitter	0.10 UIp-p max.

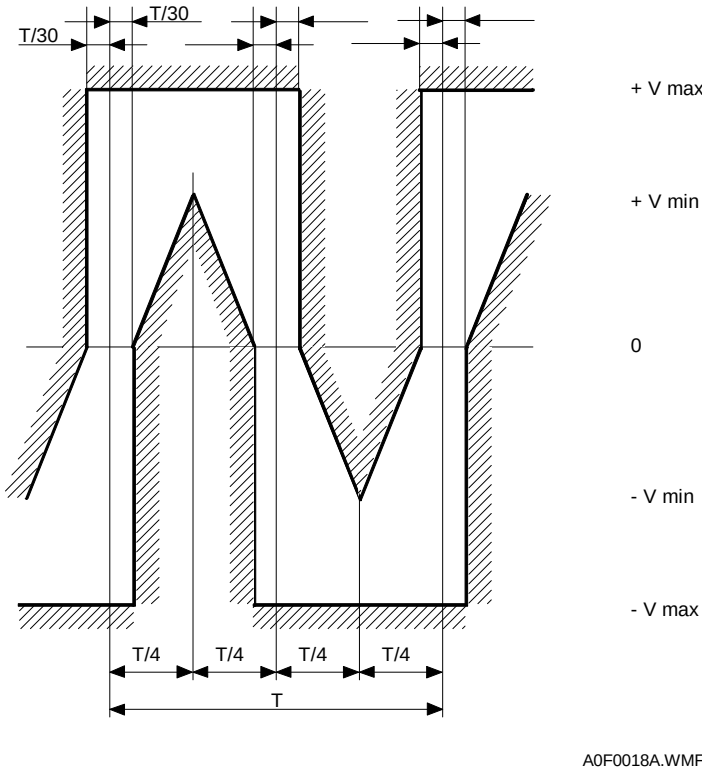


Fig. 22: Clock Output Pulse Mask at 2048 kHz

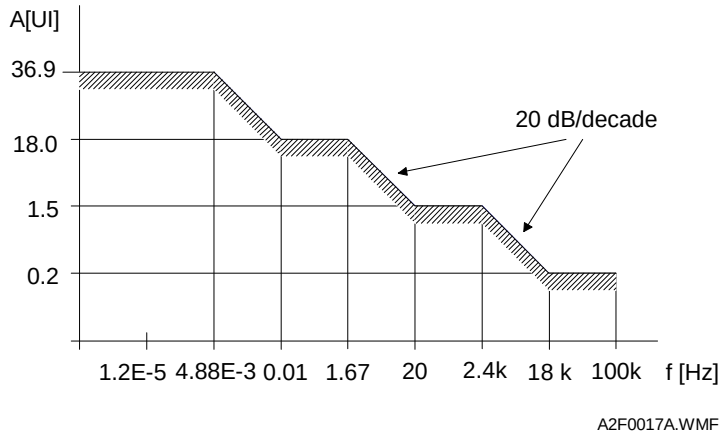


Fig. 23: Input jitter tolerance at the external clock interface at 2048 kHz

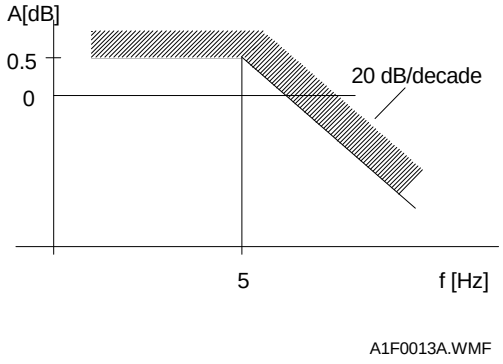


Fig. 24: Jitter transfer function from 2 Mbit/s port A to 2 Mbit/s port B or from an external clock at 2048 kHz to a 2 Mbit/s port

2.5 SXU-A Cross-Connect Unit

2.5.1 General

SXU-A is used in a Basic Node. It cross-connects n x 64 kbit/s XB-channels with possible signalling (XD-channels) as well as a limited number of n x 8 kbit/s XB-channels. SXU-A is intended mainly for network access nodes. It has a strictly non-blocking time-space matrix for 64 kbit/s signals.

SXU-A consists of a base unit and modules:

— SXU 212 cross-connect base unit
— SXZ 282 unit software module
— PDF 202 or PDF 209 power supply module

The power supply module is mounted on the base unit along with an interference emission (EMC) shield. SXU-A is 5T wide and is furnished into card slot 15. In protected mode the redundant SXU-A is inserted into slot 14.

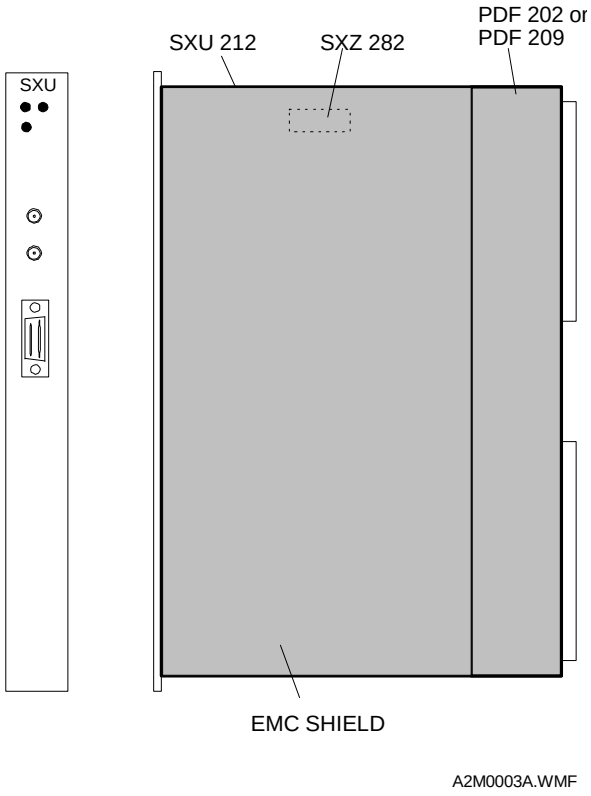


Fig. 25: SXU-A Structure

2.5.2 Operation of SXU-A

2.5.2.1 SXU-A Block Diagram

SXU-A contains two cross-connect matrices (XCM) each handling distinctive connection types. SXU's software assigns tasks to the correct XCM.

Both XCMs enter the signal coming from the DR-bus into a buffer memory. Either of the XCMs outputs an octet in each cross-connected TSB to the DT-bus.

The cross-connect capacity of SXU-A is:

— 1043 x 64 (66 752) kbit/s of n x 64 kbit/s (octet) connections (total capacity).

Out of the total capacity can be allocated:

— 32 x 64 (2048) kbit/s to n x 0.5 kbit/s (channel associated signalling) connections and

— 95 x 64 (6080) kbit/s to n x 8 kbit/s (bit) connections

When calculating the capacity of a connection, add both ends of the connection to the capacity requirement; for example the two ports in the example in Section on An Example of the Signal Cross-Connection Procedure each require one 64 kbit/s octet.

2.5.2.2 Cross-Connect Matrix 0

XCM0 connects all n x 64 kbit/s XB-channels (fully non-blocking).

The DR-bus data is written into the buffer memory, which is two frames long, using an address from the frame counter. Data is read from the buffer with an address, which itself is read from a cross-connect address memory. The unit processor writes this cross-connect address when cross-connections are created.

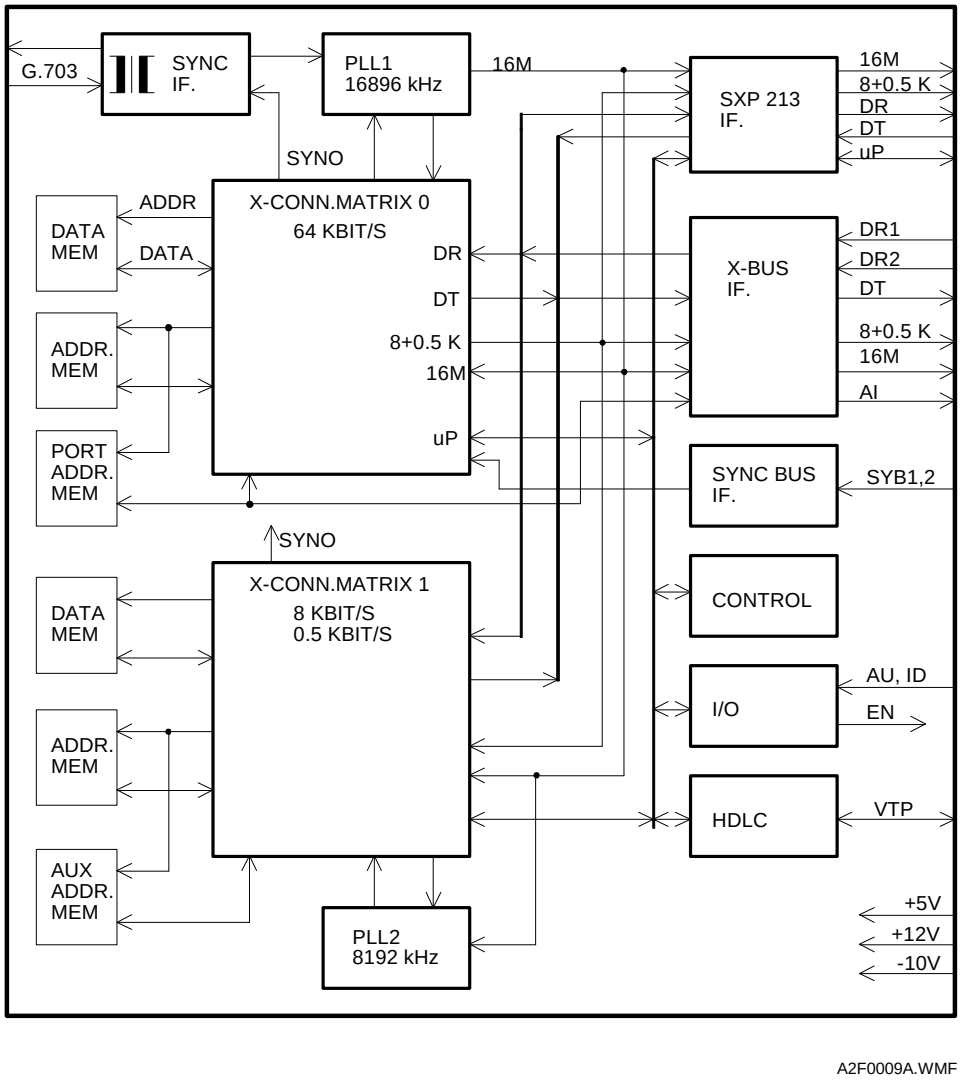


Fig. 26: SXU-A Block Diagram

In each cross-connected tsB a port address and a possible ts-address (framed interfaces) is read from a port address memory. The address is repeated in every frame. Several slow speed access interfaces in the same IF-unit can share a bus time slot, for example eight 8 kbit/s ports one tsB (subrate access interfaces at max. 4.8 kbit/s using a port rate of 8 kbit/s).

A number of ports can share an XD-time slot by using the same port address and activating themselves in only part of the frames.

XCM0 contains frame- and multiframe counters, which supply the X-bus timing. The frame- and multiframe counters of the XCM1 synchronize to the XCM0.

2.5.2.3 Cross-Connect Matrix 1

XCM1 provides n x 0.5 kbit/s XD-channel and n x 8 kbit/s XB-channel connections. Both types are connected bit-by-bit. Total capacity is 127 time slots (ts) per frame (8128 kbit/s).

Between 0 and 2048 kbit/s can be used for XD-channels (fully non-blocking). In XD-time slots the DR-bus signal is written into a two multiframes long buffer memory.

The maximum capacity for n x 8 kbit/s XB-channels is 95 ts per frame (6080 kbit/s). All ports in a node with SXU-A should be locked as uneven ports. Otherwise there may be blocking in the n x 8 kbit/s capacity.

XCM1 produces one cross-connected byte in every eighth tsB during the frame and transfers the byte temporarily into an internal buffer. All bits in a byte are processed even if some bits are not cross-connected (they are set to idle state '1'). Bytes are read from the internal buffer to the X-bus using addresses from an auxiliary address memory. XD-bytes are read from the buffer in tsB 528 to 559.

2.5.2.4 Unit Control

The SXU unit processor links to the subrack control bus via an HDLC-controller. The SXU stores cross-connection commands and port parameters of IF-units in a non-volatile memory. The unit restores its state should a power loss occur.

The non-volatile memory has 128 kbytes for saving cross-connection data and port parameters. Cross-connections can be repeatedly deleted and entered without capacity overflow. 128 kbytes of non-volatile memory is reserved for program code, which can be down loaded. The core of the program code is stored in an EPROM.

A 16-bit processor runs at 16 MHz. The processor has access to the cross-connect matrices and the cross-connect memories without interfering with the existing connections. A watchdog monitors the operation of the processor.

2.5.2.5 Power Supply

SXU-A employs the unit power supply module PDF 202 or PDF 209. The switching power supply provides three regulated output voltages: +5 V, + 12 V and - 10 V.

A redundant SXU can be inserted into or removed from the subrack while the subrack operates normally. This is accomplished by a two-phase power-up procedure, where the subrack’s auxiliary power is employed first until the SXU’s own power supply provides a stable output.

2.5.2.6 New features of SXU-A V5.0

Main oscillator

The new oscillator was designed to work within ±10 ppm through temperature range. The clock has also a hold-over feature.

Strapping

All strapping has been removed. The external clock connector symmetrical cable shield is permanently tied to the ground.

Unit software

The compatible Unit Software version is V10.0 or newer.

2.5.3 SXU-A Front Panel

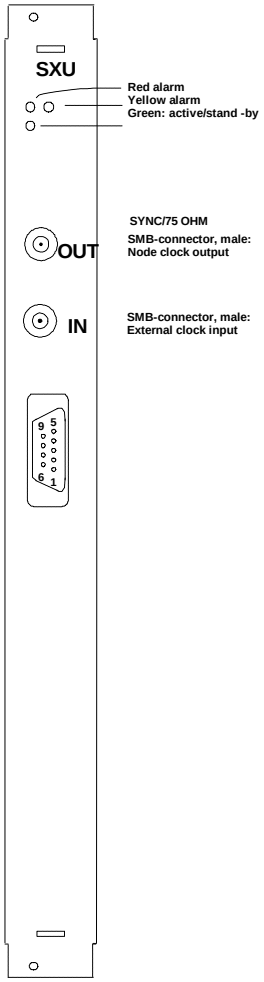


Fig. 27: SXU-A Front Panel

The figure above shows the led functions. A 75 Ω coaxial interface and a 120 Ω symmetrical interface for an external clock input and the node clock output have been provided. Either the coaxial or the symmetrical interface can be operated at a time.

SXU-A Pin Usage

Pin	Signal
1	Ext clock input, B
2	Ext clock input, A
6	Cable shield input
3,7,8	Gnd
4	Node clock output, B
5	Node clock output, A
9	Cable shield output

2.6 SXU-B Cross-Connect Unit

2.6.1 General

SXU-B is used in a Basic Node. It is intended for network transit nodes requiring extensive use of n x 8 kbit/s connections. SXU-B has a strictly non-blocking time-space matrix for 64 kbit/s signals. SXU-B cross-connects n x 64 kbit/s XB-channels with possible signalling (XD-channels) as well as a limited number of n x 8 kbit/s XB-channels. It also provides n x 64 kbit/s- and XD-channel connection.

2.6.1.1 SXU-B Structure

SXU-B consists of a base unit and modules:

— SXU 218 cross-connect base unit
— SXZ 282 unit software module
— PDF 204 or PDF 209 power supply module
— SXP 213 cross-connect module

The base unit is similar to SXU 212 used in SXU-A but equipped with mechanics 10 T wide. SXU-B is mounted in card slot 14 and the redundant SXU-B into slot 12.

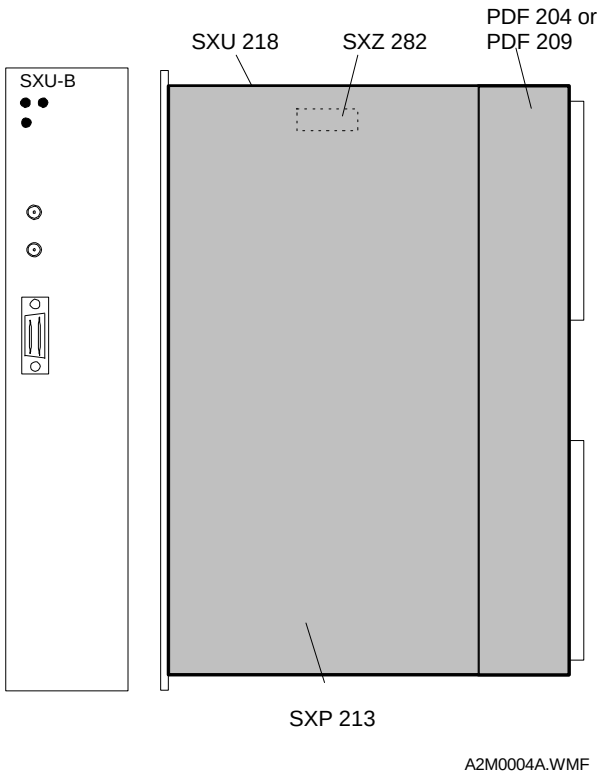


Fig. 28: SXU-B Structure

2.6.2 SXU-B Operation

2.6.2.1 SXU-B Block Diagram

SXU-B consists of a base unit SXU 218 and a cross-connect module SXP 213. SXU 218 is electrically similar to SXU 212 (SXU-A). The SXP 213 module contains seven cross-connection matrices (XCM). In SXU-B all XCMs operate in parallel to provide the required 8 kbit/s cross-connect capacity.

The cross-connection capacity of SXU-B is:

— 1043 x 64 (67 264) kbit/s of n x 8 kbit/s (bit) connections (total capacity)

Out of the total capacity can be allocated:

— 64 x 64 (4096) kbit/s to n x 0.5 kbit/s (channel associated signalling) connections

Cross-Connect Matrices 0 and 2 to 8

XCM0 and XCM2 to XCM8 connect n x 8 kbit/s XB-signals. Each matrix supplies cross-connected data bytes to the X-bus regularly in every eighth tsB. The first byte is available in tsB10 from XCM0, next byte in tsB11 from XCM2 etc.

XCM0 outputs the X-bus timing and the port addresses. Other XCMs are synchronized to the XCM0.

Cross-Connect Matrix 1

XCM1 provides non-blocking connection of up to 64 x 64 kbit/s XD-channels (total 4096 kbit/s).

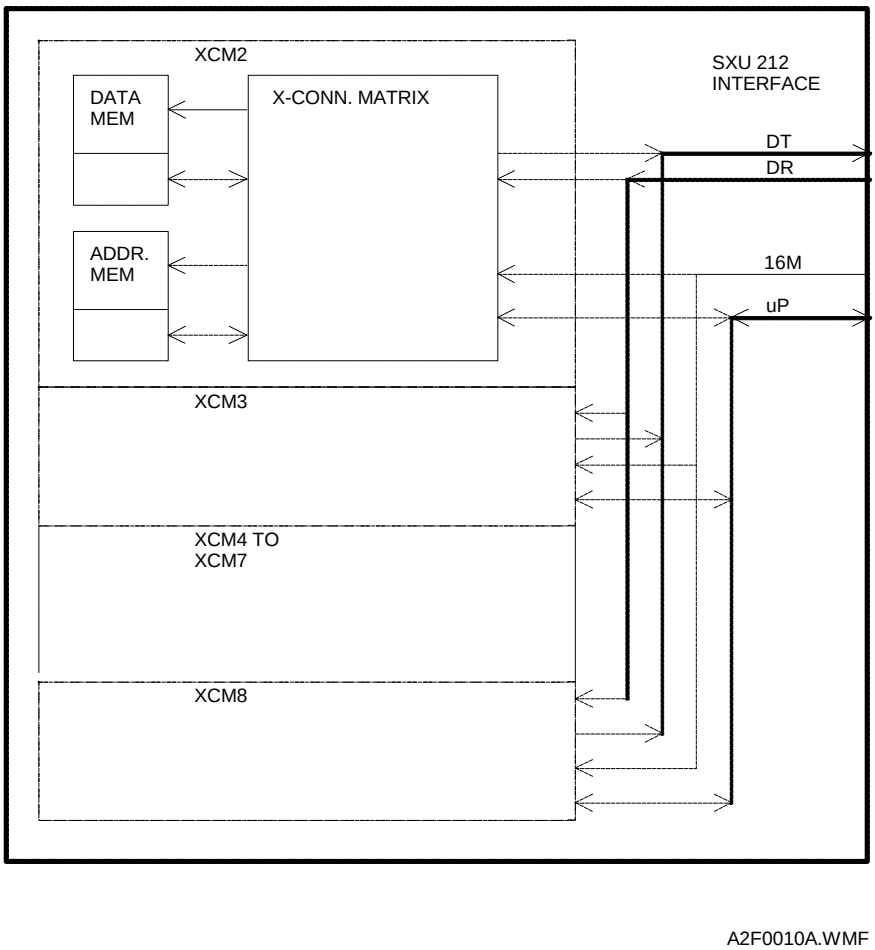


Fig. 29: SXP 213 Cross-Connect Module Block Diagram

2.6.2.2 New features of SXU-B V5.0

Main oscillator

The new oscillator was designed to work within ±10 ppm through temperature range. The clock has also a hold-over feature.

Strapping

All strapping has been removed. The external clock connector symmetrical cable shield is permanently tied to the ground.

Unit software

The compatible Unit Software version is V10.0 or newer.

2.6.3 Front Panel of SXU-B

Note: SXU-B is 10-T wide.

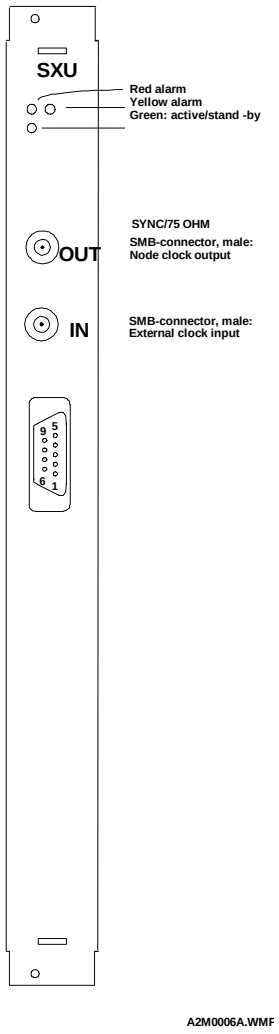


Fig. 30: Front Panel of SXU-B (10T wide)

Pin Usage

Pin	Signal
1	Ext clock input, B
2	Ext clock input, A
6	Cable shield input
3,7,8	Gnd
4	Node clock output, B
5	Node clock output, A
9	Cable shield output

2.7 XCG Cross-connection and Control Unit

2.7.1 General

The XCG is a highly integrated 5T wide unit combining the main functions of an SCU control unit and an SXU-A cross-connect unit. Additionally, a G703-75-4CH or a G703-120-4CH interface module can be installed on the XCG base unit. XCG has a cross-connection capacity of 64 Mbit/s. It cross-connects n x 64 kbit/s XB-channels with possible signalling (XD-channels) as well as a limited number of n x 8 kbit/s XB-channels. XCG is designed to operate as a part of DXX-network and can be controlled with Ericsson Network Management System.

There are four G.703 2048 kbit/s E1 interfaces, synchronization input and output as well as Service Computer interface in the front panel of the unit. XCG consists of two cards, one XCG 525 base unit which contains control processor and cross-connection features and another GDH 521/522 containing E1 interfaces (IF1-IF4) and synchronization interfaces. Interfaces 1 and 2 can be used in 1 + 1 protected mode and they support full DXX trunk interface features including management via HDLC channel in any time slots or in the TS0 spare bits. Interfaces 3 and 4 do not support management HDLC channel and can only be used as user access point (UAP). IF1 and IF2 can also be used as UAP. All four interfaces can be used in framed or unframed mode. The frame structure of the interfaces is according to CCITT G.704. For more information about G703-75-4CH and G703-120-4CH interfaces see .

XCG consists of a base unit (XCG 525) and modules:

— PDF 202 (-48 V) or PDF 209 (+24 V) power supply module
— SMZ 538 unit software module
— G.703/G.704 (75 Ω) unbalanced interface module (GDH 521) or
— G.703/G.704 (120 Ω) balanced interface module (GDH 522)

XCG unit has modular structure. The XCG unit needs to operate one piggy-back power supply unit PDF 202 or PDF 209. The width of the unit is 5T or one card slot in DXX subrack. Card slot 8 in Midi Node is reserved for the XCG unit.

Starting from the upper edge of the front panel of the unit (G703-75 or 120-4CH equipped), there are two alarm LEDs, Service Computer connector, two G.703 interfaces, SYNC input/output connectors and again two G.703 interfaces. In the back of the unit there are two 2 x 32 pin eurocard (DIN 41612) connectors. The upper euro connector is used in transmitting the LOCAL VTP bus signals, equipment alarm output signals, 5 V power to the bus interface circuits and test input/output signals. The lower connector is used in transmitting the cross-connect bus signals, the 5 V power to the bus interface circuits and the battery bus. The power supply module is mounted on the base unit.

2.7.2 XCG Operation

2.7.2.1 XCG Block Diagram

The XCG unit takes care of subrack data and timing signals, 16896 kHz main clock of node, frame and multiframe synchronization signals. The external clock reference signal for the main clock can also be connected from any IF unit in the subrack as well as from the SYNC interface. One local VTP channel, subrack alarm output signals (PMA, DMA, MEI), node inventory management, storing parameters for all IF-units - excluding GMU and FRU units - in subrack and event reporting to the NMS are main responsibilities of XCG unit. XCG cannot be protected.

The functional block diagram is presented in the following figure. The common functional blocks are:

— Cross-connect block
— Microprocessor block for control functions
— Power supply PDF 202 or PDF 209
— Interface module G703-75-4CH or G703-120-4CH

The microprocessor block, the cross-connect block, and the data interface to subrack are located on the XCG 525 board, which is the main board of the unit. The channel interfaces and the sync-interface are located on the interface module.

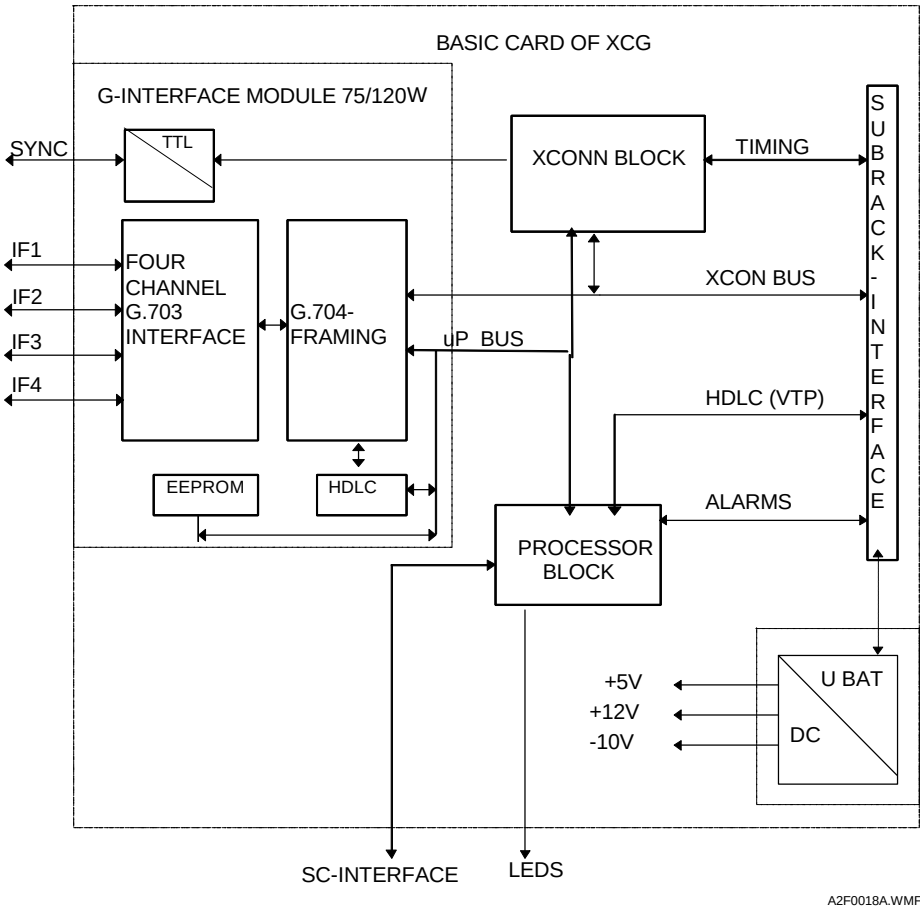


Fig. 31: 25 Functional Block Diagram

2.7.2.2 Cross-Connect Block

The cross-connect block has the following main functions:

— cross-connection of data channels
— control of the cross-connect bus
— unit's master clock oscillator
— interface for external clock I/O
— selection of a reference signal for the master clock oscillator
— selection of a clock signal for the external clock output

The cross-connection is done in the switching matrix of the cross-connect block. The cross-connection bus contains 1056 cross-connectable time slots (8-bit bytes). The bits from the interface blocks are collected by using this bus. The cross-connect switch combines the needed new bytes for the interfaces by using 8 kbit/s granularity. Usually, whole time slots or bytes are cross-connected. The delay caused by the cross-connection is one 8 kHz frame (125 µs).

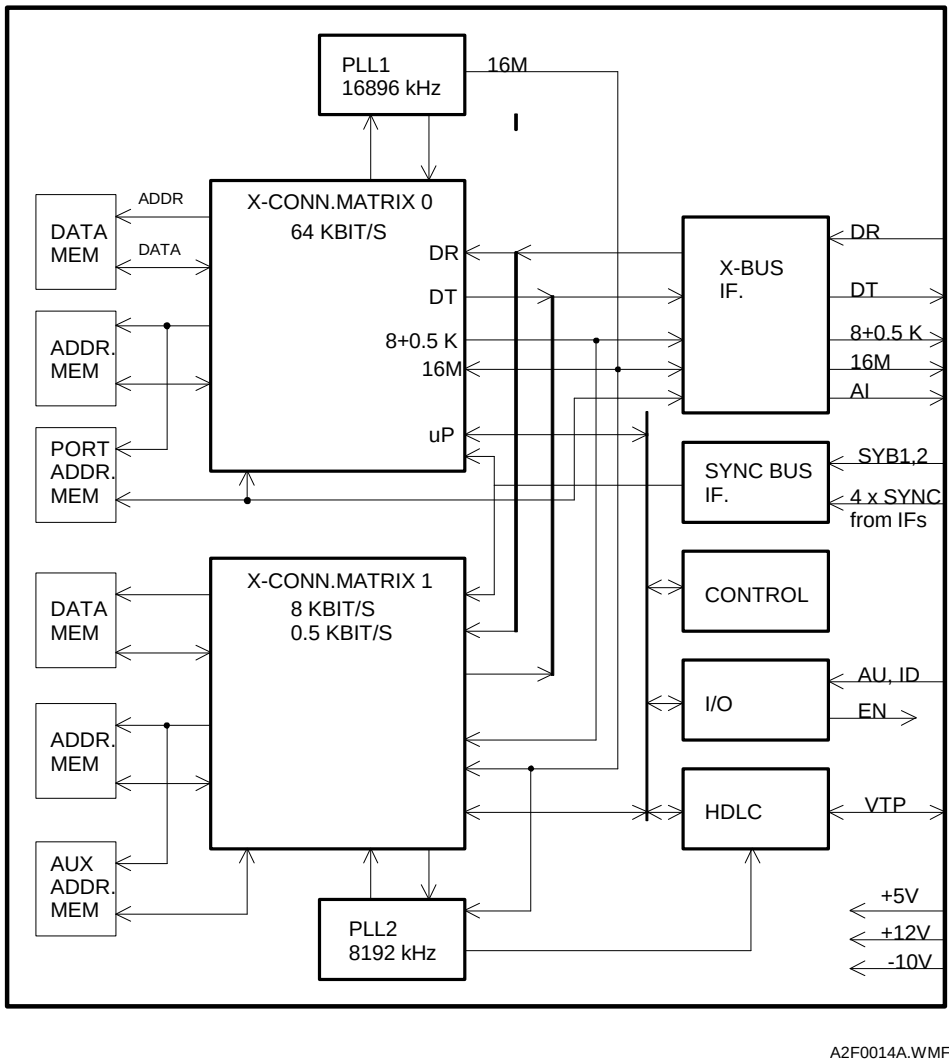


Fig. 32: The Block Diagram of XCONN block

The X-connect block exchanges data with IFs or IF-units by placing a channel address on the cross-connection bus, which activates data buffers of the corresponding channel. Rx & Tx data are carried on separate 8-bit buses.

The X-connect block supplies 16.896 Mhz master clock signal to the interface module and subrack. The Master clock is used to clock the bus operations and to create the correct frequencies for the transmitted signals.

XCG contains two cross-connect matrices (XCM) each handling distinctive connection types. XCG's software assigns tasks to the correct XCM.

Both XCMs enter the signal coming from the DR-bus into a buffer memory. Either of the XCMs outputs an octet in each cross-connected TSB to the DT-bus.

The cross-connect capacity of XCG is:

— 1043 x 64 (66 752) kbit/s of n x 64 kbit/s (octet) connections (total capacity).

Out of the total capacity can be allocated:

— 32 x 64 (2048) kbit/s to n x 0.5 kbit/s (channel associated signalling) connections and
— 95 x 64 (6080) kbit/s to n x 8 kbit/s (bit) connections

When calculating the capacity of a connection, add both ends of the connection to the capacity requirement.

Cross-Connect Matrix 0

XCM0 connects all n x 64 kbit/s XB-channels (fully non-blocking).

The DR-bus data is written into the buffer memory, which is two frames long, using an address from the frame counter. Data is read from the buffer with an address, which itself is read from a cross-connect address memory. The unit processor writes this cross-connect address when cross-connections are created.

In each cross-connected tsB a port address and a possible ts-address (framed interfaces) are read from a port address memory. The address is repeated in every frame. Several slow speed access interfaces in the same IF-unit can share a bus time slot, for example eight 8 kbit/s ports one tsB (subrate access interfaces at max. 4.8 kbit/s using a port rate of 8 kbit/s).

A number of ports can share an XD-time slot by using the same port address and activating themselves in only part of the frames.

XCM0 contains frame- and multiframe counters, which supply the X-bus timing. The frame- and multiframe counters of the XCM1 synchronize to the XCM0.

Cross-Connect Matrix 1

XCM1 provides n x 0.5 kbit/s XD-channel and n x 8 kbit/s XB-channel connections. Both types are connected bit-by-bit. Total capacity is 127 time slots (ts) per frame (8128 kbit/s).

Between 0 and 2048 kbit/s can be used for XD-channels (fully non-blocking). In XD-time slots the DR-bus signal is written into a two multiframes long buffer memory.

The maximum capacity for n x 8 kbit/s XB-channels is 95 ts per frame (6080 kbit/s). All ports in a node with XCG should be locked as uneven ports. Otherwise there may be blocking in the n x 8 kbit/s capacity.

XCM1 produces one cross-connected byte in every eighth tsB during the frame and transfers the byte temporarily into an internal buffer. All bits in a byte are processed even if some bits are not cross-connected (they are set to idle state '1'). Bytes are read from the internal buffer to the X-bus using addresses from an auxiliary address memory. XD-bytes are read from the buffer in tsB 528 to 559.

2.7.2.3 Microprocessor Block

The control microprocessor block contains the following functional units:

— Microprocessor
— Memory
— HDLC channel
— A/D conversion
— Service Computer Interface

Microprocessor

The unit is controlled with a 16-bit microprocessor. The processor has access to the cross-connect matrices and the cross-connect memories without interfering with the existing connections. A watchdog monitors the operation of the processor.The system program is stored on the board in two interchangeable EPROM memories. The application programs are stored in non-volatile FLASH memories; it is thus possible to update these programs from NMS. The non-volatile memory is also used to store the unit's operating parameters, the unit serial number, cross connection data info, port parameters and the parameters of all IF units in the node. In the case of a power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parameterization. The RAM memory of the processor operates as a working storage containing e.g. error counters and data buffers for the HDLC links and the frame control bus. The microprocessor supports system-level testing.

Memory

The 512 kbyte non-volatile memory is for saving cross-connection data and port parameters as well as program code. Cross-connections can be repeatedly deleted and entered without capacity overflow. The core of the program code is stored in an EPROM. Memory is implemented with surface mount components.

— 256 kBytes RAM
— 512 kBytes Flash memory
— 256 kBytes of EPROM

HDLC Channel

The XCG unit processor links to the subrack control bus via an HDLC-controller. The XCG stores cross-connection commands and port parameters of IF-units in a non-volatile memory. The unit restores its state should a power loss occur.

A/D Converter

The unit includes a multichannel analog-to-digital converter (ADC) which monitors the operating voltages, auxiliary voltages 1 and 2 of subrack and control voltage of the master oscillator.

Service Computer Interface

The XCG unit has a single asynchronous serial channel. This interface is used on service computer connection (CNF1). The baud rate of the UART is 9600.

2.7.2.4 Power Supply

The unit receives its operating voltage from the power supply module. There are two models of power supply available, PDF 202 for -48 V battery input and PDF 209 for +24 V battery input. The modules can be replaced as a whole and plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The module provides the operating voltages +5V, +12V and -10V. The module also receives a +5V bus voltage, which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset circuit and a low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

2.7.2.5 Interface Module

Four-channel G.703 interface module is intended to be used with a XCG base unit. There are two alternatives of the unit, one for a 75 Ω unbalanced interface, G703-75-4CH and another for a 120 Ω balanced interface, G703-120-4CH. The modules include four independent E1 transmission channels to carry data and also to provide an internal communication link of the DXX system. The function of the module is to convert signals received by XCG base unit of a DXX node so that they comply with G.703 specifications and other relevant recommendations concerning the electrical interface towards equipment outside the DXX network. The G703 module also converts signals from other equipment into signals acceptable to the DXX network. Transmission channel interfaces are independent of each other. The frame structure is in accordance with G.704 for 2048 kbit/s. Two interfaces can be used for DXX trunk connections with a 1+1 protection possibility and all four interfaces can be used as user access points. See chapter G703-75/120-4CH Interface Module for details.

2.7.2.6 Internal Buses

Cross-Connect Bus Structure

Cross-connect bus functions are also monitored by the interface units. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. The interfaces monitor the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing the interface unit will activate the Bus Sync Missing alarm.

XCG is continuously testing the XCON bus by transmitting test patterns in TS 1053.

The cross-connect bus covers unit positions 2 to 8 in the Midi Node.

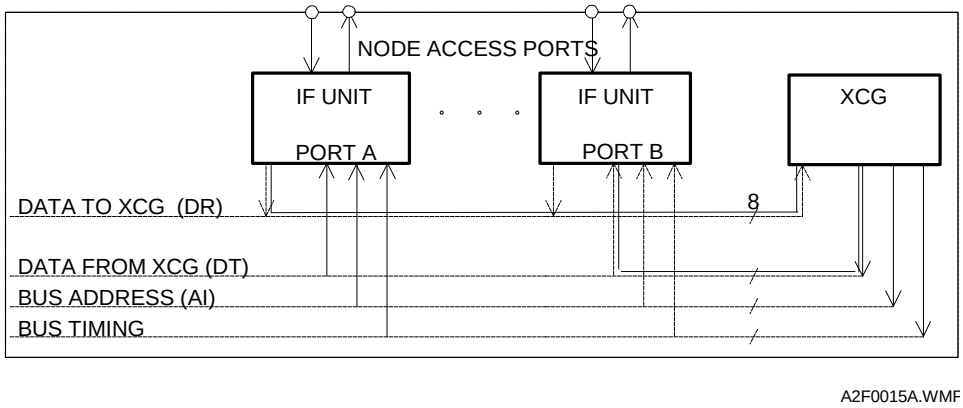
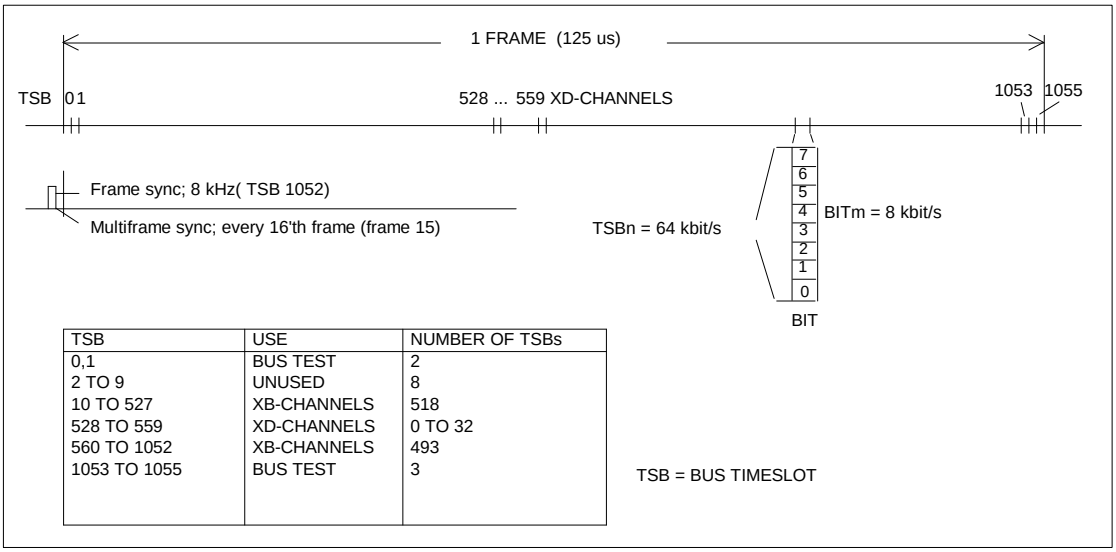


Fig. 33: X-Bus Signals

The X-bus operates synchronously. Interface units (IF-units) adjust mesochronous or plesiochronous access port signals into the X-bus by bit buffering. IF-units with a frame structure also buffer the frame (multiframe) phases.

XCG supplies the bus clock (16896 kHz), frame timing (8 kHz) and multiframe timing (0.5 kHz). XCG generates a port address for each cross-connected bus time slot. A port exchanges a data byte with XCG when the port recognizes its address. Ports with a frame structure receive the frame time slot number explicitly.



TSB	USE	NUMBER OF TSBs
0,1	BUS TEST	2
2 TO 9	UNUSED	8
10 TO 527	XB-CHANNELS	518
528 TO 559	XD-CHANNELS	0 TO 32
560 TO 1052	XB-CHANNELS	493
1053 TO 1055	BUS TEST	3

Fig. 34: Logical Structure of the X-Bus

The X-bus frame is divided into 1056 bus time slots (tsB) numbered from 0 to 1055. Each tsB has a capacity of 64 kbit/s. Each of the eight bits in a tsB can be considered as a separate 8 kbit/s channel. Up to 32 tsBs can be further multiplexed by the 16 frames long multiframe for XD-channel cross-connection. The XD-time slots are cross-connected bit-by-bit creating n x 0.5 kbit/s channels.

Five time slots are reserved for node monitoring. The remaining 1051 bus time slots are reserved for cross-connection of user data.

X-Bus Allocation

X-bus capacity is allocated by the XCG software based on selected port parameters. Ports are classified as even and uneven ports. XCG supports uneven allocation. 2048 kbit/s ports get an uneven allocation if receive buffer is 4 or 8 frames. An uneven port does not reserve tsBs for XB-channels until the time slots are cross-connected. A possible XD-time slot is reserved when the port is locked. More than 32 uneven 2048 kbit/s ports can be accommodated in a node, if part of the time slots are not cross-connected and if the signalling capacity is not limiting.

2.7.2.7 An Example of the Signal Cross-Connection Procedure

64 kbit/s XB-Signal Connection

The following sequence details the procedure when XCG cross-connects a byte between two 64 kbit/s ports. Fig. 33 shows the data path in the direction from port A to port B (dashed line).

When the operator locks the port parameters the port is automatically allocated one tsB. The operator creates a cross-connection between the two ports.

In each bus frame for ports A and B:

— XCG outputs the port's address on the address bus
— XCG reads a cross-connect address from an address memory and using the address reads a data byte from the data memory
— The port and the XCG exchange a data byte
— XCG writes the byte it received into a data memory
— The port sends the byte it received to the access interface. The delay of XB-channels in the XCG is one frame (125 µs). The total delay through a node also includes the buffer delays in the IF-units.

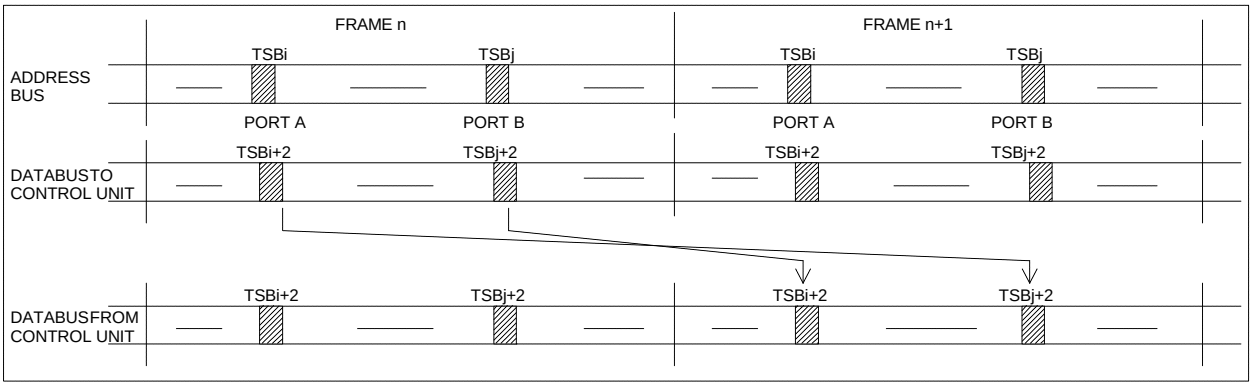


Fig. 35: Data Byte Exchange on the X-Bus

8 kbit/s XB-Signal Connection

The data exchange on the X-bus is similar to that of the 64 kbit/s signal. A whole byte is always transferred. XCG assembles the byte bit-by-bit during eight consecutive time slots. Bits, which have not been cross-connected, are set to idle state '1'. Signal delay is one frame within the XCG.

0.5 kbit/s XD-Signal Connection

The procedure is similar to the 8 kbit/s connection, but here the multiframe structure is employed. The delay in the XCG is one multiframe (2 ms).

X-Bus Interface

XCG supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

XCG exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. From the XCG the base units receive the time slot address which directs the bus data transmission to one selected time slot at a time.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and, therefore, able to extract the payload data channels and to map them into desired locations. The frame alignment signals repeated at regular intervals divide the transmitted data into frames which have a defined structure for each transmission speed. In the DXX system the frame repetition frequency is always 8 kHz so that frames of different length, i.e. frames containing a different number of bits, must be used for different transmission speeds. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronization is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure.

The CRC check sum is used to check the reliability of the synchronization by counting how many error-containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called simulating frame synchronization word.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels which are added to the framed signals. The unit processor can transmit and receive messages to/from other nodes with a two-channel HDLC controller connected to both framed interfaces of the unit. Usually the messages are sent via the control bus to the other units where they are processed or through which they are sent to other nodes. The transmission speed of the HDLC channels can be selected within the limits of 4 kbit/s to 64 kbit/s, depending on the requirements and the available transmission capacity.

In addition to the frame synchronization words and the transmitted data channels, the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organisation can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.

The frame structures are described in Appendices.

2.7.2.8 VTP Control Bus

The XCG unit has an interface for internal VTP control bus. The VTP bus is used for communication between the units within one subrack. The bus is synchronous serial high-speed local area network with data and clock lines and interface circuits. The bit rate of the local VTP bus is 2 Mbit/s.

VTP is an abbreviation from the words Virtual Token Protocol which is a collision-free media access method based on the token passing principle implemented by the aid of timers. The logical link control is based on LLC3 protocol in both buses. The upper layer protocols are the same as the those of the external management interfaces of DXX nodes. The local VTP bus supports unit addresses 1…31.

2.7.2.9 Node Clock System

The main oscillator (PLL1) runs at a frequency of 16896 kHz. Accuracy in internal timing mode is + 30 ppm over the operating temperature range. For jitter and wander specifications, see Chapter 2.7.5. The main oscillator can be locked to an external source or to the received clock of an access interface. Two synchronization buses are provided for transferring clocks to the XCG.

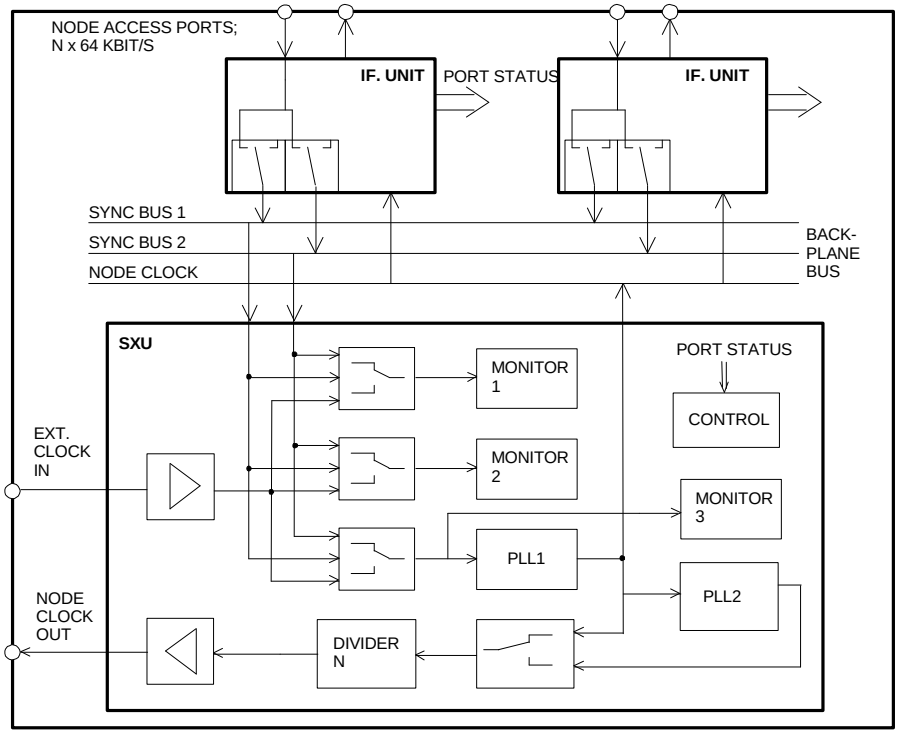


Fig. 36: Node Clock System

Auxiliary Oscillator

An auxiliary oscillator (PLL2) is locked to the PLL1 providing frequencies in the 2048 kbit/s hierarchy for the clock output interface. Frequency of oscillation is 8192 kHz. PLL2 also supplies the 2048 kHz clock used for connection to the subrack control bus VTP and Tx-clock for GDH IFs.

Fallback List

In a DXX network trunk lines and the XCG's external clock interface are normally used to transfer timing to the node. While the node clock can be synchronized from interfaces at lower rates (n x 64 kbit/s), it should be noted that synchronization from 2 Mbit/s and 8 Mbit/s signals results in better controlled wander properties.

The operator selects in the Master Clock-menu of the Node-window ports for the fallback list and assigns their priority. Up to five ports can be entered. The XCG selects the highest priority port with a non-alarm status as the input to the main oscillator.

Clock Monitoring and Alarms

XCG monitors the clock selected and also the next choice on the fallback list. The external clock is monitored when enabled.

Fallback list clocks are also monitored by the interface units. By a major fault in a port's rx-signal, the IF-unit clamps the clock (on SYNC BUS 1/2) and sends a clock status message to the XCG. XCG's monitoring circuit opens the phase-locked-loop maintaining the clock frequency until the processor selects another clock. Internal timing is selected if all clocks on the fallback list have failed.

2 Mbit/s interfaces with a frame structure can employ a dedicated bit in the frame as a clock far end alarm bit (FEA). It is used on trunks transferring timing between nodes. If an intermediate node in a network loses its synchronization, the alarm bit is transmitted from all its interfaces. The receiving node's IF-unit then clamps the clock on sync bus 1/2.

After a fault is cleared the IF-unit gradually clears the clock status. The operator can enter a clock acceptance time in the Master Clock-menu. A clock is not selected again until its status has been good over the acceptance time.

XCG supervises that the PLL1 is locked to the clock source. A phase-locked-loop alarm is generated if the source frequency is out of range or if it contains jitter more than specified in Technical Specifications.

Clock Output Interface

Node clock output is provided at the external interface in the XCG interface module (G703-75/120-4CH). The output is activated and its frequency selected from the Master clock window. The output control function, when set to on state, disables the output when the XCG is in internal timing or locked to the external interface. When output control is off, clock output is active regardless of the fallback list state.

2.7.2.10 Clock Faults Monitored in the XCG

Fault description	Status	Led	Alarm message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock on fallback list and missing	MEI	Red	Loss of external clock
External clock on fallback list, clock interface disabled	PMA	-	External clock warning
Locking to a clock failed	PMA	Red	Phase-locked-loop alarm
Main oscillator fault in XCG	PMA	Red	X-connect RAM fault
Clock far end alarm (individual for each link)	MEI	Yel	Clock far end alarm

If the node clock supplied by the XCG should fail, the GMH/GCH-units transmit an independent clock with a basic frequency tolerance to output ports. Node clock alarm is generated by the IF-units.

2.7.2.11 Node Level Operations

The software of the XCG takes care of the following node-level operations:

— Node Inventory Management
— Backup of unit settings
— Rack alarm (PMA, DMA, MEI) control
— Event reporting to the Network Management System
— Channel test loops

Node Inventory Management

The Node Inventory Management software includes functions to get and set node and subrack identifications, to create and delete inventory, to add and remove units, to get inventory reports and to monitor the presence of registered or unregistered units. The Create Inventory operation is used to register all existing units for the inventory. The Add Unit operation is used to register a given unit for the inventory. The Delete Inventory makes all units unregistered - in other words, all units are removed from the inventory. The Remove Unit operation is used to remove a given unit from the inventory.

The Inventory Report provides the node and subrack identification data and the list of existing or registered units. The Installation Error fault condition is detected if the inventory data is not unambiguous and consistent. The Missing Unit fault condition is detected if a registered unit is not present. The Extra Unit fault condition is detected if there is an unregistered unit present in the subrack.

Backup of Unit Settings

The XCG unit stores the backup settings of all registered units for possible unit replacements excluding GMU and FRU units. A new replacement unit will inherit the backup settings of the unit registered for the unit slot. The checking of compatibility of settings is based on hardware and software types.

The backup settings are updated to the XCG unit when a unit is registered or when the settings of the unit have been changed. The backup settings are copied from the XCG unit when a registered unit is replaced by another compatible unit.

Rack Alarm Control

The XCG unit controls the three LEDs and the corresponding relay outputs for the equipment alarms (PMA, DMA, MEI) of a subrack. The rack alarm LEDs and the corresponding relay outputs are located in the PFU or PAU units. The rack alarms, PMA, DMA, MEI, are given if any unit in the subrack has an

active fault condition which requires the corresponding alarm as a consequent action. The XCG unit collects PMAs, DMAs and MEIs from the units of the subrack and sums them separately for each rack alarm.

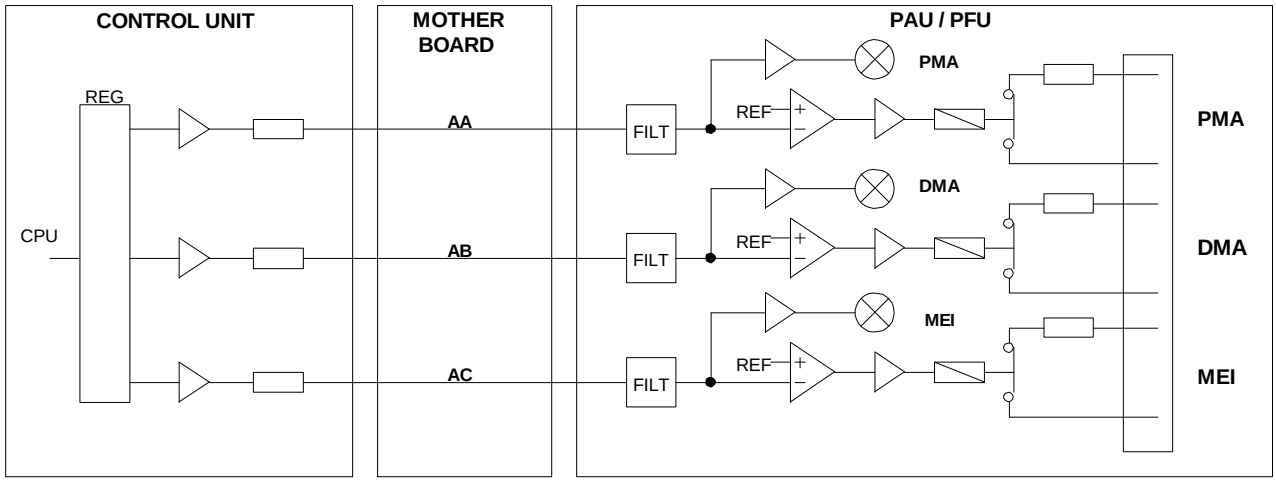


Fig. 37: Rack Alarm Control

Rack alarms can be delayed. The rack alarm delay can be set (0…600 seconds) by the user. A summed alarm must be active at least for the set delay time - not necessarily continuously - before the rack alarm is activated in PFU or PAU. The rack alarm will be passivated in PFU or PAU when the summed alarm has been continuously passive for at least the set delay time.

The rack alarm PMA and DMA can be cancelled. The rack alarm cancellation is not delayed. When PMA and DMA have been cancelled, MEI is activated as a reminder.

Event Reporting to Network Management System

The XCG unit does not only supervise the registered units of the subrack for the rack alarms but also to support subrack-level status polling from the centralized Network Management System as well. The node state report contains the status of the subracks which are not in the normal state.

The subrack state report contains the status of the units which are not in the normal state. For example, all changes in fault conditions and configuration are indicated for all units. These reports make it possible to get detailed information from the correct units for different purposes.

While the subrack state report is created, the route to the polling DXX server is updated to the local routing table of the XCG unit from the invoke message. This route can be used to send spontaneous event reports to the DXX Server. The unit reporting modules can send event reports to the local XCG unit which then sends them to the DXX Server. The most important application is the reporting of trunk fault changes in the trunk recovery management.

2.7.2.12 Interface Unit and Module Combinations

Midi Node can be equipped with several interface units which are used for external trunk and channel connections. These are application-specific depending on the trunk and channel requirements. Depending on the use of common units (control and cross-connection units and power units) and the redundancy requirements of the application, there are 4 to 6 interface unit slots available in a Midi Node Subrack

RXS-S8. Node capacity is not determined solely on physical space, but memory and processor capacity must also be considered. The maximum cross-connect capacity of one Midi Node is 64 Mbit/s. This means that the total amount of bandwidth for the interface ports within one node cannot exceed 64 Mbit/s.

Interface units are used for line and user interfaces. Units are designed as single, double, or triple width cards, depending on their functionality. The actual DXX trunk and channel interfaces are defined by the interface module that resides as a subassembly on the base unit. Different kinds of interface modules can be mounted on the same base unit.

An XCG Multifunction unit equipped with G703-75/120-4CH interface module is an interface unit as well as a control and cross-connection unit for the whole Midi Node. Other available interface unit and module combinations for use in a Midi Node are listed below.

Interface Unit and Module Combinations

Interface Units

Modules	**XCG**	**GMM**	**VMM**	**GMH**	**GCH-A**	**VCM-5T**	**VCM-10T**	**CAE**	**AIU 1:1**	**AIU 1:4**
G703-75/120-4CH	x									
T1		x								
X21-G704-S			x	x						
V35-G704-BS			x	x						
V36-G704				x						
G703-75				x						
G703-120				x						
G703-8M				x						
OTE-LP				x	x					
OTE-LED				x	x					
LTE				x	x					
BTE-4096				x						
BTE-2048				x						
BTE-2048-2W				x						
BTE-1088				x						
BTE-384				x	x					
BTE-64					x					
V24-DCE						x				
V24-DCE-PMP						x				
V24-DTE						x				
V35-IEC						x				
X21						x				
G703-64						x				
V35							x			
V36							x			
PCM-10VF								x		
ADPCM-10VF								x		

Interface Units

Modules	XCG	GMM	VMM	GMH	GCH-A	VCM-5T	VCM-10T	CAE	AIU 1:1	AIU 1:4
EM-2*10								x		
STM-1-IO-13									x	x

In addition, the following interface units are available for Midi Node, but they contain no separate interface modules:

— IUM-5T
— IUM-10T
— ISD-LT/ISD-NT
— CCS-PCM
— CCO-PCM
— CCS-ADPCM
— CCO-ADPCM

Moreover, there are three server units which can be used in a Midi Node:

— ECS
— EPS
— EAE

2.7.2.13 G703-75/120-4CH Interface Module

General

Four channel G.703 interface module is intended to be used with XCG base unit. There are two alternatives of the unit: one for a 75 ohm unbalanced interface, G703-75-4CH and another for a 120 Ω balanced interface, G703-120-4CH. The modules include four independent E1 transmission channels to carry data and also to provide an internal communication link of the DXX system. The function of the module is to convert signals received by XCG base unit of a DXX node so that they comply with G.703 specifications and other relevant recommendations concerning the electrical interface towards equipment outside the DXX network. The G703 module also converts signals from other equipment into signals acceptable to the DXX network. Transmission channel interfaces are independent of each other. The frame structure is in accordance with G.704 for 2048 kbit/s. Two interfaces can be used for DXX trunk connections with 1+1 protection possibility and all four interfaces can be used as user access points.

Interface Module Operation

Mechanical Design

The mechanical design of the four-channel G.703 interface module is based on the standard DXX system mechanics. The module can be installed to an XCG base unit.

Operating voltage is fed to the module from the base unit through the same connectors that are used for signals for the control microprocessor bus and for the data transmission processing.

Power Supply

A module receives its operating voltage from the base module. The module requires the operating voltage of +5V.

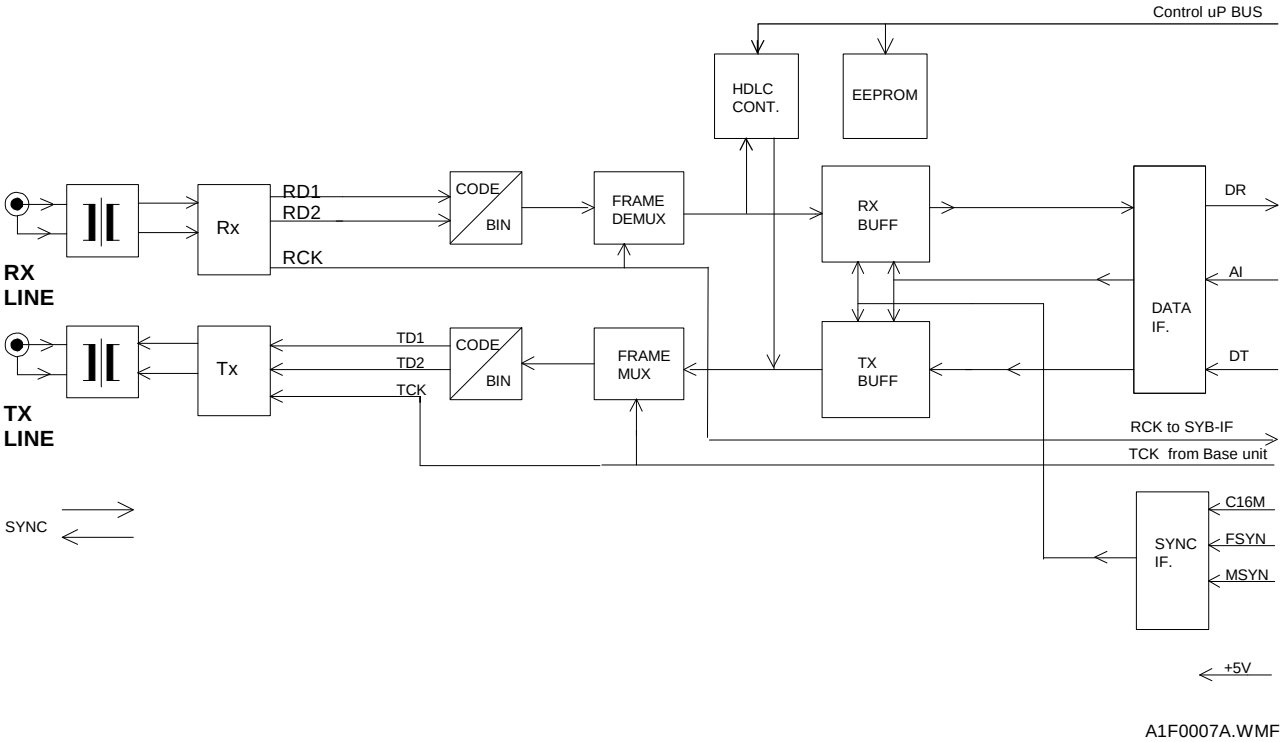


Fig. 38: Functional Block Diagram for one channel of the G703-75/120-4CH module

Control Processor bus
The interface module is controlled with a microprocessor located on the base unit. A non-volatile memory on the base unit is used to store the module's operating parameters so that in the case of a power interruption the module is automatically reset to the conditions prevailing before the interruption, without specific parameterization. EEPROM that is located on the module carries the serial number of the module, HW-version and module ID.

Line Interfaces
The four channel module is connected to a transmission line through interface circuitry. The block contains the analog components required for the E1 interface.

In the receiving direction the interface module regenerates the coded signal received from the transmission line and transforms the signal to the digital level. The module monitors the level of the received signal; if it is too low or completely missing, the module sets an AIS signal to the base unit and at the same time it activates a missing signal alarm through the processor bus. The behaviour is according to G.775.

Because the line interface provided by this module fully complies with all relevant recommendations, a complete specification of this interface is given under Technical Specifications only. The following briefly describes the line interface circuit design of the G703-75/120-4CH module.

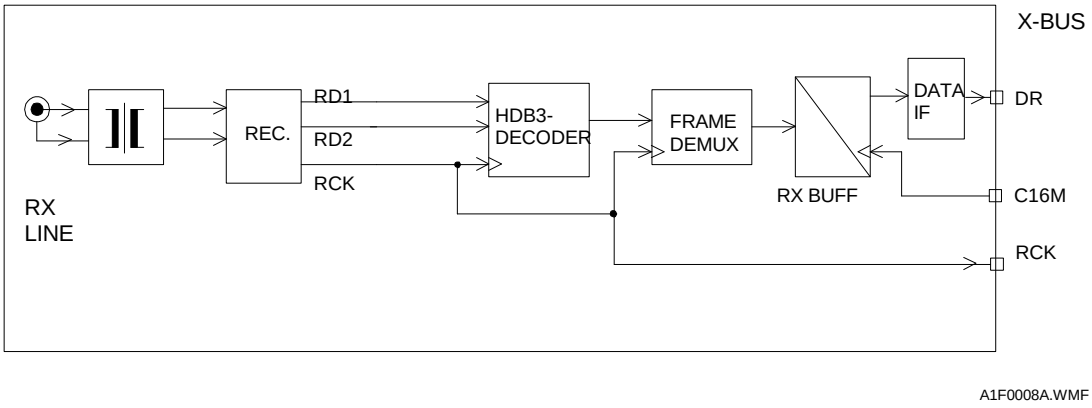


Fig. 39: Data and Clock Processing in the Receiving Direction

The receiving direction clock which is recovered from the data in the interface module is used to decode the line code and to demultiplex the frame. If there is no received signal, the interface module replaces the received clock with the transmitted clock.

The received clock from any of the four channels on the interface module can be connected to the two SYB buses on the base unit to be used as the node synchronization signal. The clock to the SYB-bus is disconnected if there is a received signal failure.

The module generates the frame structure and the G.703 line code for the data in the transmitting direction. The transmitting direction 2.048 MHz clock and C16M node clock received from XCG are phase-locked to each other.

In the Receive direction the line transceiver regenerates CMOS level RD1, RD2 and RCK from analog Rx signal. The input transformer together with resistors match the line impedance and amplitude for the line transceiver circuit. Diode limiters protect against overvoltage.

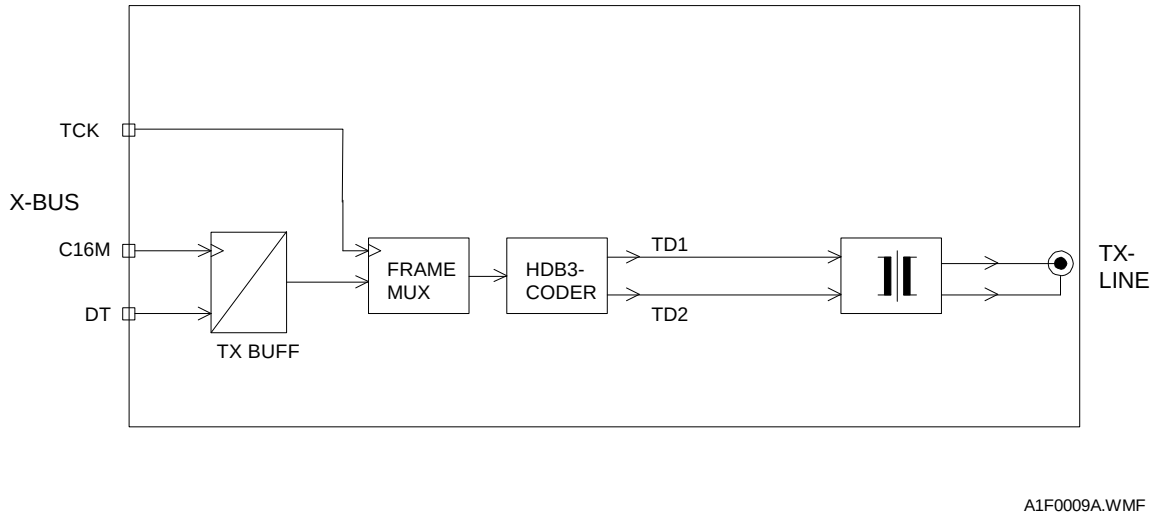


Fig. 40: Transmitting Direction Clock and Data Generation at 2048 kbit/s

The transmitting direction clock for 2048 kbit/s is generated by the crystal oscillator of the base unit. The oscillator is locked to the C16M clock of the bus, which is used to create the frame and to generate the output pulses in the coder.

In the transmit direction the CMOS level HI-active positive and negative pulses are fed to the line transceiver which produces pulse shape according to G.703 recommendation together with the line transformer and resistors. Output impedance matching to the line is also accomplished with the transformer and resistors. Diode limiters protect against overvoltage.

Clock Interfaces

An input interface for an external clock and an output interface for the node clock are provided. The interfaces comply with the ITU-T rec. G.703 § 10. Connectors that are the same type as the interface connectors are located in the front panel. For interface specifications see Chapter 2.7.5.

Functional Structure

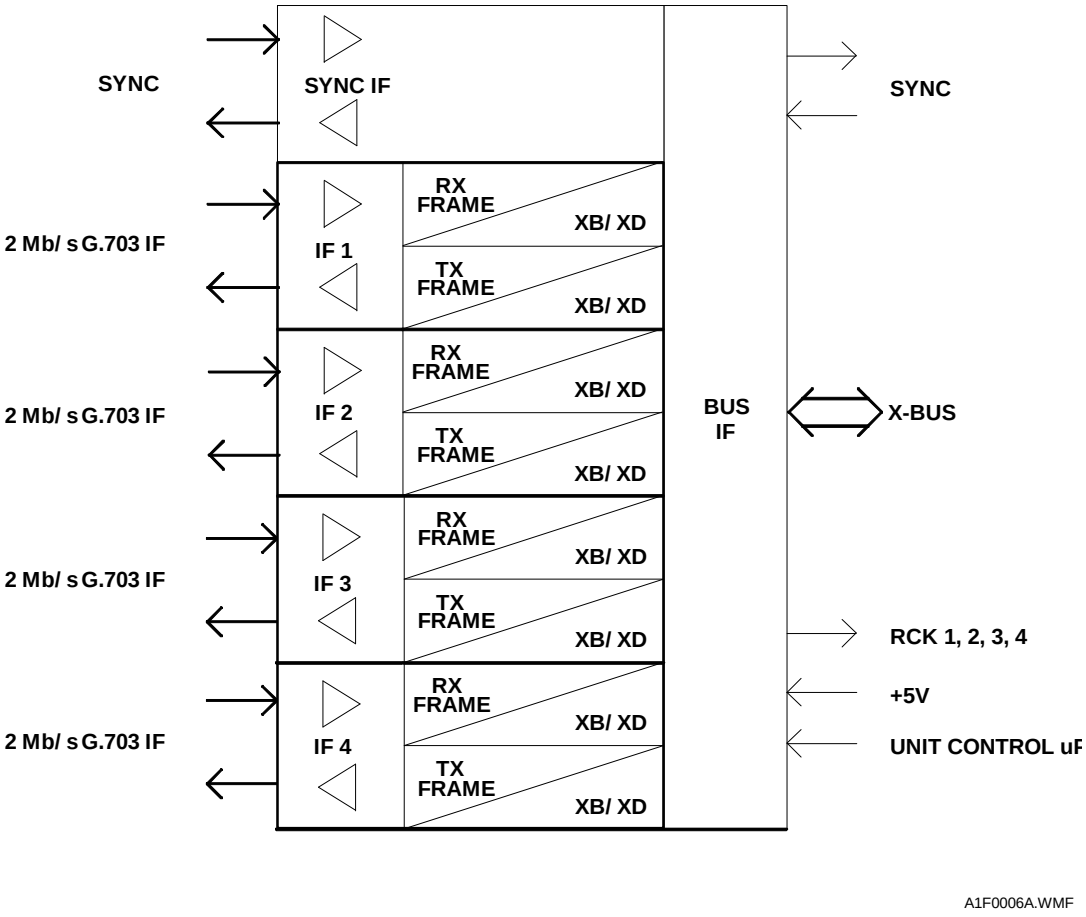


Fig. 41: Functional Structure of G703-75-4CH and G703-120-4CH modules

The main functional blocks of the G703-75-4CH and G703-120-4CH modules include line interfaces for four channels, channel frame multiplexer and demultiplexer circuits, channel output and input buffers, and an X-bus interface common for all channels.

The processor on the base module controls and monitors the functions of the interface module. Information related to control and monitoring is transmitted on an internal control bus of the subrack from the base unit. Through this control bus the base unit can communicate with other units in the subrack. The processor generates HDLC messages and processes HDLC messages received from framed interfaces.

The data transmission channel interfaces convert analog G.703 line signals to/from signals suited for the module's digital circuits. In the receiving direction a signal attenuated by the transmission line is regenerated and the clock signal is recovered. The payload signal and the clock signal are transformed to a level suitable for the digital logic. The line interfaces are realized at the same printed circuit board.

The framed signal which is carried on the transmission line is assembled and disassembled in the Tx-frame and Rx-frame blocks of each channel. In the transmitting direction the Tx-frame block creates a signal by mapping data from the X-bus into correct time slots, adding frame alignment signal bits and the CRC check sum, and by generating the HDLC channel at a required position within the frame, with the aid of the processor. Line transceiver converts digital Tx signal to analog signal at the line interface. In the receiving direction the line interface block converts analog signal to a digital signal. The Rx-frame block searches the received signal for the frame synchronization word. When the synchronization is found, the Rx-frame block can extract the data transmission time slots, check the CRC check sum, and recover and supply the HDLC channel to the processor. The frame structure is in accordance with G.704 / 2048 kbit/s. If required, it is also possible to remove the framing and have the channel to operate in a transparent mode.

The transmit buffers of the channels are used to store data received from the cross-connect through the X-bus, so that there is always a time slot available for transmit by the Tx-frame block. The transmit buffers also synchronize the phase of the transmitted frame with the phase of the X-bus and stuff idle data in unused time slots of the frame.

The receiving buffers of the channels store incoming data so that the required time slots are always available to the cross-connect module. These buffers also form a flexible buffer in order to compensate for minor momentary speed differences between the X-bus and the received signal. The length of the receiving buffers can be changed in accordance with the application's requirements. For instance, in some cases a minimum connection delay is required, and in plesiochronous operation slips are desired to occur as seldom as possible.

The X-bus interface transfers signals from the X-bus to the channels, timing signals and control information to the module, and correspondingly it transfers data and monitoring information from the channels to the X-bus.

X-Bus Interface
The base unit supplies the C16M clock for the interface module. The incoming C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The base unit supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface module by placing a channel address on the X-bus. This activates the data buffers of the corresponding channel of the interface module. Received and transmitted data is carried on separate 8-bit wide buses. Through the base unit the G703-75/120-4CH module receives the time slot address which directs the bus data transmission to one selected time slot at a time.

Bus functions are monitored by the interface module. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and therefore able to extract the payload data channels and to map them into desired locations. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronization is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure. The latter method is used by G703-75/120-4CH modules.

The CRC check sum is used to check the reliability of the synchronization by counting how many error containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called simulating frame synchronization word.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels, which are added to the framed signals. The base unit processor can transmit and receive messages to/from other nodes with a HDLC controller connected to interfaces 1 and 2. Usually the messages are sent via the control bus to the other units where they are processed or through which they are sent to other nodes. The transmission speed of the HDLC channels can be selected within the limits of 4 kbit/s to 64 kbit/s, depending on the requirements and the available transmission capacity. In the G703-75/120-4CH modules the interfaces 1 and 2 are equipped with HDLC channels.

In addition to the frame synchronization words and the transmitted data channels, the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organisation can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.

The frame structures are described in Appendices.

Buffers

In the transmitting direction the buffer supplies time slot data from the X-bus to the frame to be transmitted. When the cross-connect unit supplies data to the X-bus, it also adds information about the location in the transmitted frame where the data is to be placed. The unit stores the data in its transmit buffer in a position corresponding to the time slot's position in the frame. The frame multiplexing circuits will fetch the data when they are transmitting the corresponding time slot. As it is possible to write the data from the bus to any time slot position in the buffer, the buffer must control that write and read operations do not simultaneously address the same time slot. In the G703-75/120-4CH modules the transmit buffer length is set to two frames. Then the frame multiplexing block reads the first frame area and the bus writes into the second frame area. This transmit buffer arrangement causes a delay of one frame or 125 μs.

In the receiving direction the buffer supplies received time slot data from the demultiplexed frame to the X-bus. When the XCG cross-connect block requests data from the interface module through the X-bus, it also specifies the time slot concerned. Usually, the phase of the received frame does not coincide with the frame phase of the X-bus; on the other hand, the receiver writes time slot data into the Rx buffer clocked by the received frame. Therefore the Rx buffer has to control that the read and write operations do not collide, in spite of speed fluctuations and jitter. If the read and write addresses come too close, one of them has to be moved, i.e. centred. The allowed minimum distance between the read and write addresses depends on the system requirements. In the interface module the centring is made by changing the read address, the change being always one frame or a multiple of a frame. The centring causes a certain number of frames to be lost or re-transmitted; the number is proportional to the distance which the read address is moved. Through the user interface it is possible to select four different lengths for the receiving buffer, in order to meet different requirements, such as a minimum delay or the ability to tolerate large speed fluctuations.

Centring is required when the equipment is powered up, when a received signal contains disturbances, or when the transmission is plesiochronous. If a plesiochronous system constantly exhibits a frequency difference in the same direction, the buffer has to be centred at regular intervals. The length of the interval depends on the frequency difference and on the distance from the centred read address position to the position where a new centring occurs.

Operating Modes of Buffers

Rx Buffer	Rx delay	Tx length	Tx delay
4 Fr	1…3 Fr	2 Fr	1 Fr
8 Fr	1…7 Fr	2 Fr	1 Fr

4 Fr Rx Buffer

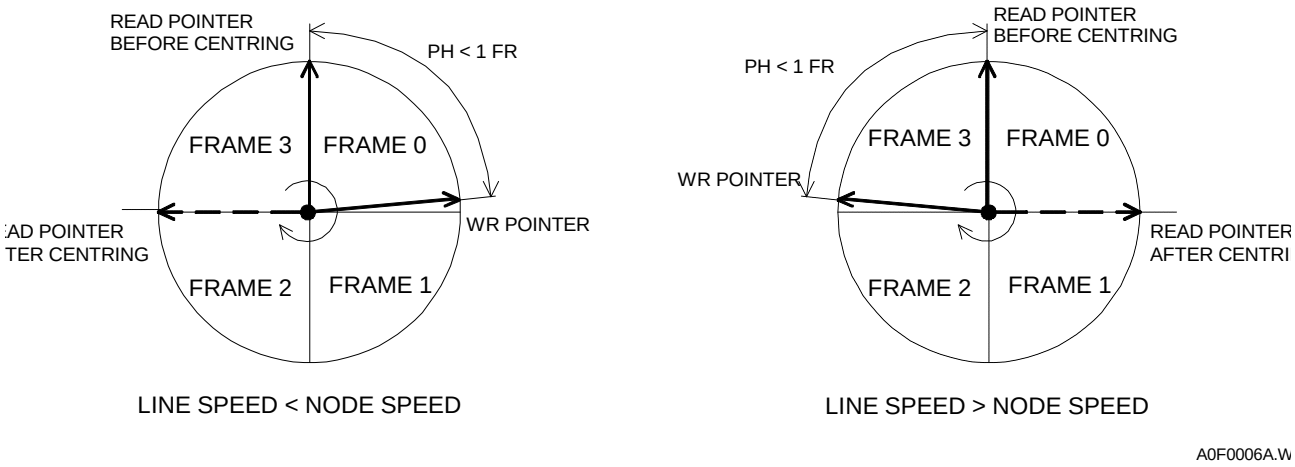


Fig. 42: Centring in an Rx Buffer of Four Frames

The minimum allowed distance between the read and write addresses is one frame. The distance is checked at intervals of four frames when the read address moves to frame Fr0 (from the frame Fr3). If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. The address jump direction depends on the direction from which the write address was closing in on the read address. Centring means here that one frame is either lost or repeated once. In a plesiochronous system with a four-frame Rx buffer the interval between centring situations is: at 2048 kbit/s 256/df.

8 Fr Rx Buffer

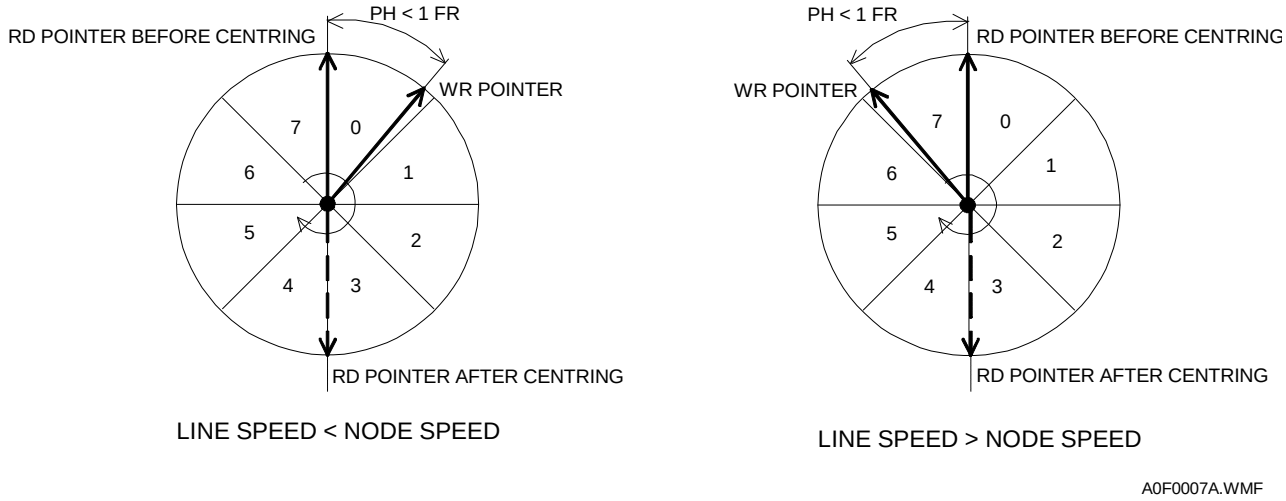


Fig. 43: Centring in an Rx Buffer of Eight Frames

The allowed distance between read and write addresses in an Rx buffer of eight frames is one frame. If a shorter distance is detected by the check, then the read address is moved to a new position four frames farther away. In this case centring means that four frames are either lost or repeated once. The eight frames buffer retains the frame alternation also after the cross-connect, when a 2048 kbit/s framing structure is used.

In a plesiochronous system the interval between centring situations is: at 2048 kbit/s 1024/df

Multiframe Buffers

In the transmitting direction the signalling data is directed through the same buffer as the time slot data. The signalling multiframe of the frame to be transmitted is synchronized to the multiframe clock of the X-bus. The cross-connect unit supplies frame signalling data together with other time slot data of the frame. The interface module generates a synchronization time slot in the first frame of the signalling multiframe. Thus the signalling data and time slot data have equal delays in the transmitting direction.

In the receiving direction the phase of the received signal multiframe usually differs from the phase of the X-bus multiframe. Thus the received signalling data has to be buffered until the cross-connect unit performs the cross-connect function for the concerned data.

Multiframe Buffers

Frame buffer mode[a]	Multiframe buffer mode[b]	MFr-Rx delay	MFr-Tx delay
4…8 frames	2 MFr	0…2 MFr	1 Fr

a The length of a frame is 125 µs.

b the multiframe length is 2 ms.

The centring is triggered if the distance between the received multiframe phase and the X-bus multiframe phase is less than one frame. In a buffer with two multiframes the centring is made by moving the write address one multiframe further, which means that the information of one multiframe is lost or repeated.

In interface module and cross-connect unit the time slot data and signalling data have separate buffers. Therefore there are different delays in the processing of signalling data and time slot data. This means that the signalling data and time slot data which are placed in a transmitted frame do not necessarily originate from the same frame.

G703-75/-4CH Interface Module Operating Modes

Trunk interfaces and user access interfaces are the two categories of DXX node interfaces. Trunk lines are lines connecting the DXX nodes, and the trunks are always framed interfaces. The interface module supports full DXX trunk features at interfaces 1 and 2. User access interfaces connect lines from users to a node. The user access interfaces can be channel interfaces or framed channel interfaces. The user interface presents a G.704 framed channel interface to the user. The most important difference between the trunk mode and the user mode is that the use of time slots in the trunk interface is determined by the Network Management System whereas the use of time slots in a framed channel interface is determined by the user. All interfaces on the module can be used as user access ports.

2048 kbit/s Trunk

When a line is used as a trunk line, a part of the frame is dedicated to transfer internal system information. This information will contain data on e.g. network management channels that use the HDLC format. The transmitter will always regenerate the frame synchronization word and the CRC check in a trunk line.

The framing and CRC check have to be selected when a trunk line connection is established. The corresponding HDLC channel has to be activated and bits B5…B8 in time slot ts0 are recommended bits for the link. The trunk buffer is short in order to ensure minimal delay through the node. It is recommended to activate the signalling time slot CAS of the trunk so that it is always reserved for signalling and not used as a data time slot by the Network Management System.

Split Trunk Lines

A split trunk line can be used to combine several parallel 2048 kbit/s interfaces in order to increase the maximum number of time slots of a n x 64 kbit/s trunk interface. The time integrity of the time slots in the split trunk line is preserved even if the 2048 kbit/s is connected through physically separated cables. The split trunk mode can be used when a frame with CRC4 is used. The split trunk mode always requires long buffers (eight frames). One of the interfaces will function as a master and the others as slaves. All split components must have the same bit rate.

The interfaces are synchronized to each other by their CRC4 multiframe structure. In the transmitting direction the interface transmit buffers and Tx-frame multiplexers are synchronized with the X-bus MSYN signal to transmit in the same multiframe phase. In the receiving direction the master interface sends information about its receiving buffer read phase to the slaves, which will center their own receiving buffers to the same phase. This operation causes data time slots sent from a transmitting node in the same frame to be read together within one frame into the cross-connect unit of the receiving node.

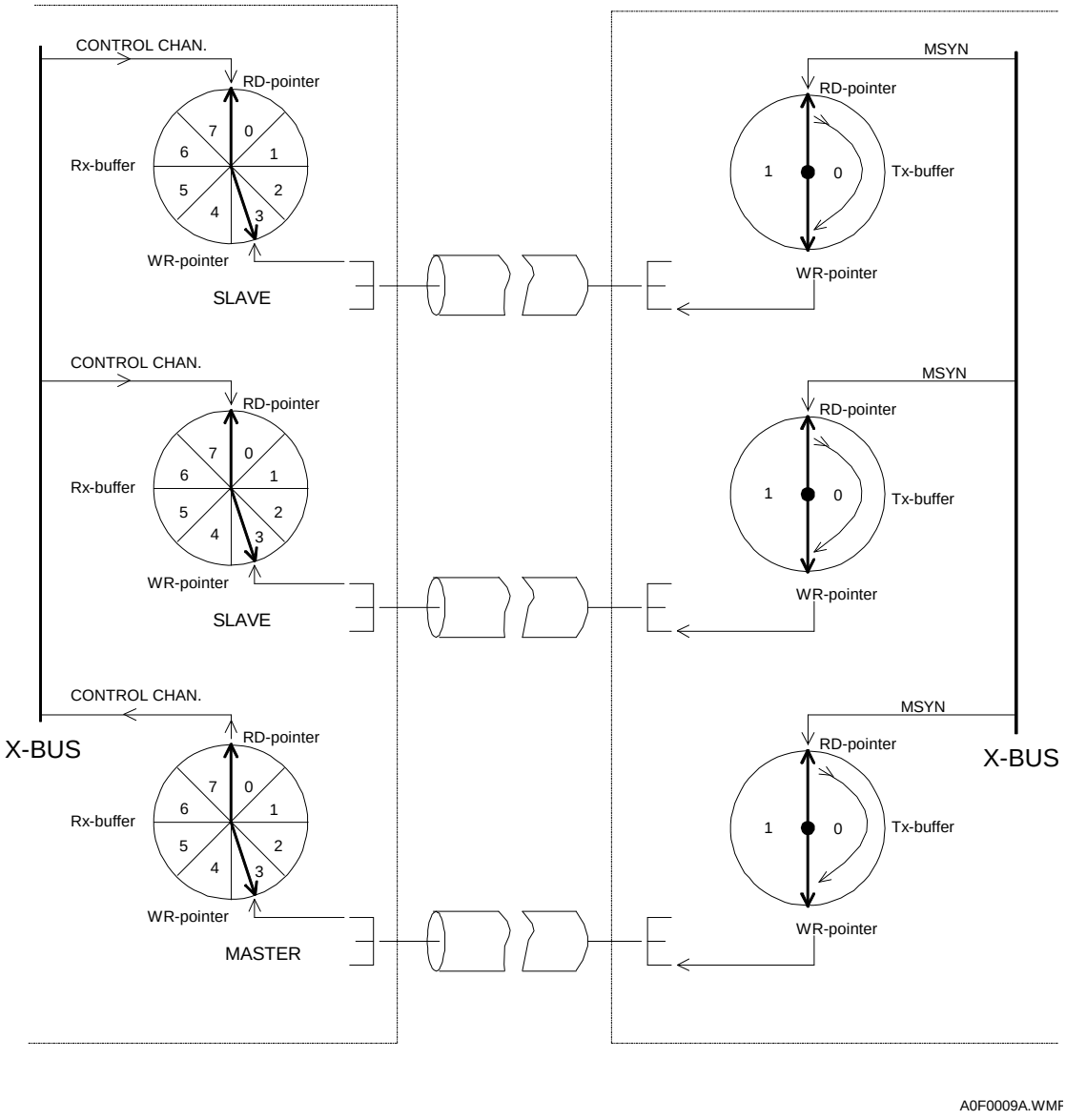


Fig. 44: Split Trunk Line Operating Principle

Theoretically, the maximum delay allowed between lines in a split trunk line is 0.5 frames: due to the centring the master read address occurs when the write address is in the area 6…2. Due to technical reasons, however, the maximum delay is 50 µs.

Each line of a split trunk line will handle its own signalling data. Those lines which carry one or more data channels with signalling data will use the last time slot or ts16 if it is possible as a signalling channel with a multiframe structure. It is not necessary to use a CAS time slot for lines that do not include data channels with signalling.

Interface module as User Access Point

The interface module can provide a G.704 framed channel interface to the user. The framed user access point has the same features as a corresponding trunk interface. The special bits are used in accordance with customer requirements. There are many possibilities to use the interface module as a user access point. Some examples are discussed below.

Framed; With or Without CRC

This is the basic way to connect pieces of equipment which use the G.704 frame structure to a DXX node. Only the data channels in time slots ts1…ts31 is transmitted over the network together with signalling data in the time slot ts16, if required.

The framing structure is demultiplexed at the interface point and only payload data will be supplied to the cross-connect system for further processing. In the transmitting direction the whole framing structure and the frame synchronization word are created in the interface and payload data from the cross-connect is added to the frame. The user equipment to be connected has usually no information about the protocol of the DXX system control channel. Therefore the HDLC channel will not be connected to the interface (with the exception of some DXX system modems). The free bits in time slot ts0 can be set to a state required by the user equipment. The synchronization remote end alarm indication bit RAI may be used, if required by the equipment to be connected. It is recommended to use the CRC check in the interface when the user equipment supports the use of CRC. Some equipment use the CRC E bits in a way not conforming to standards and in such cases unnecessary alarms can be avoided by setting the bits in a fixed state, usually 1.

When individual channel signalling is used, the multiframe structure in the receiving direction is demultiplexed in the interface and the signalling for each channel is transferred to the cross-connect for further processing. In the transmitting direction the multiframe synchronization time slot is created in the interface and stuffed with free bits. Signalling data from the cross-connect is placed into the signalling time slot. The free bits usually have the Permanent 1 state. If no signalling is used, then also time slot ts16 may be used to transmit payload data.

Framed; Transmission of Free Bits in ts0 Through the Network

It is possible to transmit the free bits of time slot ts0 through the DXX network when the equipment connected to a DXX node can utilize these free bits. Other functions may be the same as in the previous example. The free bits of time slot ts0, which are utilized by the application and transmitted through the network, are set to the X-conn state when the GDH (interface) module parameters are defined. The unit will then transmit these bits in the same state as it receives them from the cross-connect. Accordingly, bits received in time slot ts0 are supplied to the cross-connect in the same state as they are received.

On the transmission line the data transmission capacity is 4 kbit/s for one free bit in time slot ts0 due to the frame alternation. The total data transmission capacity of all five bits B4…B8 is thus 20 kbit/s. However, the DXX system utilizes a format where one free bit of time slot ts0 uses a capacity of 8 kbit/s on those connections on which it is transmitted through the network. Thus, a total capacity of 40 kbit/s is required to transmit all bits B4…B8 through the network. Transmission of the free bits of time slot ts0 always uses 64 kbit/s of the DXX node internal X-bus capacity for each interface, regardless of the number of transmitted bits.

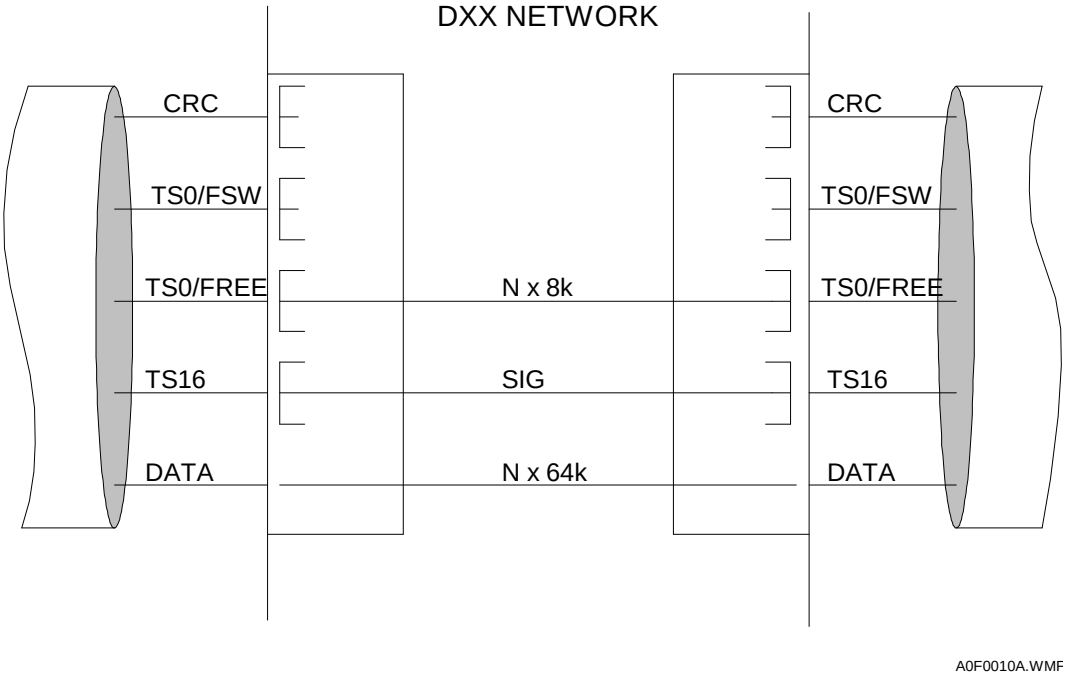


Fig. 45: TS0 Free Bits Connected Through the Network

Framed; Transmission of Time Slot ts0 Through the Network

It is possible to use the frame synchronization word to monitor the complete connection through the DXX network. In this case the whole time slot ts0 is directed via the cross-connect and transmitted to the far-end equipment. In this case the frame synchronization word, the free bits of time slot ts0 and the frame remote end alarm are transmitted over the whole connection. If it is required to connect signalling data separately over this connection, then the CRC check has to be regenerated in the user access interface. A new CRC check sum has to be calculated because the frame contents will change due to the different treatment of signalling data and normal data. The CRC check may be inactivated when the user equipment does not support the use of CRC.

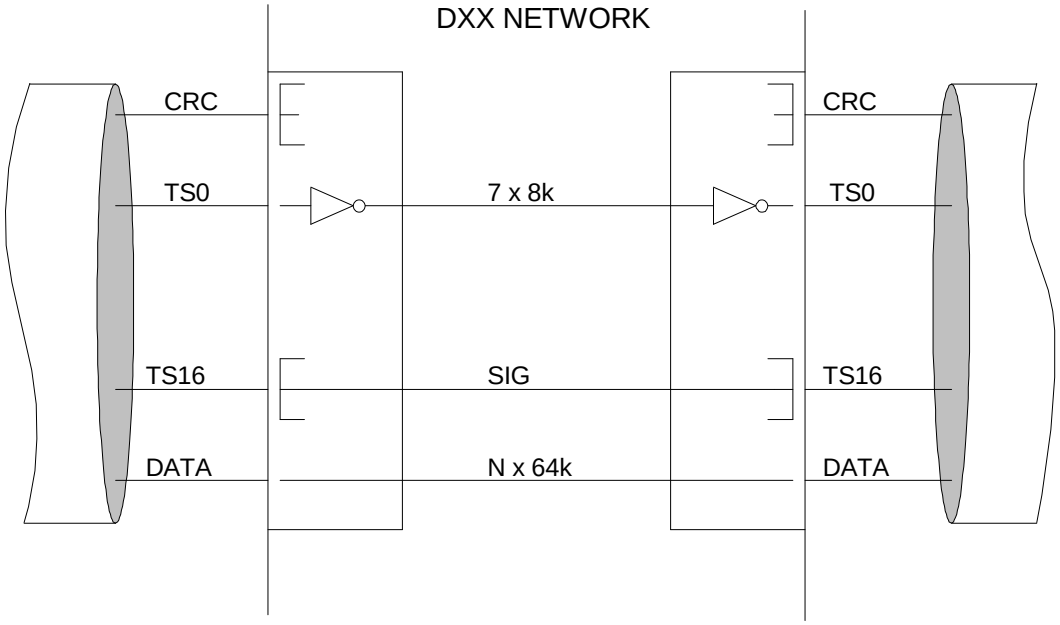


Fig. 46: TS0 Connected Through the Network

When it is connected to the transmission network, the time slot ts0 is inverted in the receiver before it is forwarded to the cross-connect. The time slot is in the inverted state when it is transmitted through the network, and in the far-end user access interface it is again inverted into its original format and then added to the frame as the synchronization time slot. The time slot ts0 is inverted so that it cannot cause false synchronization of the trunks when it propagates through the network. A trunk capacity of 56 kbit/s is used in order to transmit the whole time slot ts0 through the network. The transmission of the time slot ts0 uses 64 kbit/s of DXX node internal X-bus capacity for each interface.

When the interface parameters are set (during commissioning), the Fault consequence BER 10E-3 should be set Off. This causes received data with a bit error rate worse than 10E-3 (calculated with the aid of the frame synchronization word) to be connected through the network, and not to be set AIS as in normal transmission.

When the time slot ts0 is transmitted through the network, he user access interface will respond to errors in a way that is different from the normal. The remote end frame level alarm bit is not activated when the user access interface receiver detects a serious frame error, because this error will cause the remote end user equipment to respond, e.g. through the AIS, and to activate the remote end alarm bit. The remote end alarm bit is then transmitted back to the near-end user equipment. Moreover, the interface module will not respond to a received FrFEA bit. If an interruption occurs in the transmission network and an AIS is given instead of a payload signal to the interface, then this condition will be detected in the transmitter and an AIS is sent to the user equipment. The interface simultaneously activates the AIS from X-bus alarm.

Framed; Ts0 and CRC Connected Through the Network

It is possible to monitor the quality of the user's connection over the whole network with the aid of the CRC check. To enable this, a combination of the time slot ts0 and the CRC check is sent through the network from the near-end user equipment to the far-end user equipment. The CRC check sum is calculated for the total signal. In order to get equal results in the unit creating the CRC check sum and in the unit evaluating the CRC check sum, all bits must have the same state at both locations. The receiver will receive signalling data and payload data through different delays, and therefore it is not possible to use cross connected channel signalling, if the CRC check is transmitted over the connection. The idle data of possibly unused time slots has to be the same at both ends of the connection.

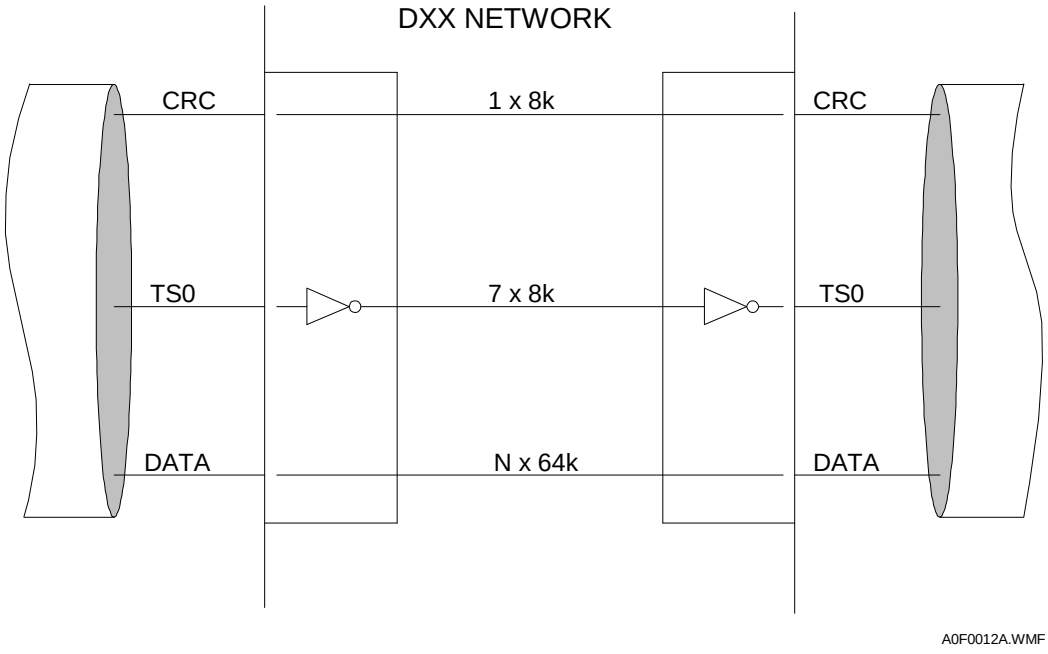


Fig. 47: TS0 and CRC Connected Through the Network

The time slot ts0 is inverted before it is transferred to the transmission network. A capacity of 64 kbit/s is used on a trunk line to transmit the combination of time slot ts0 and the CRC check, and 64 kbit/s of the internal DXX node cross-connect bus. CRC check E-bits indicating remote end block errors are also connected through the network. If these bits are not used they must set to the state 1. The interface responds to errors in the same way as when only time slot ts0 is connected through the network.

Transparent Without Frame

The interfaces of the module can also operate in a transparent mode. In this mode the received signal is connected through the network without any manipulations. The receiver is not synchronized to the incoming signal frame structure; no additions to the output signal are made in the transmitter. However, the receiver does cut the signal into slices of eight bits, which are transmitted through the network and from these slices a signal conforming to the original signal is then reconstructed in the receiver. In the transmission network a transparent signal requires a capacity according to its interface bit speed.

In order to use the interface in the transparent mode the interface parameter Framing must be set Off during parameterization. No frame errors are detected in the transparent mode, as the frames are not processed in any way. An alarm for error rate 10E-3 will be calculated only from code errors, whereas the error rate in a normal mode is calculated using also frame synchronization word errors.

Transparent With CRC Monitoring

The interface can be set to a function mode, in which the signal is transparently connected through the network, but in which the user access interface receiver synchronizes to the received signal frame structure and performs a CRC check on the signal. In the transmit direction the signal contents is not changed. The interface is set into this mode by defining the Framing parameter as CRC monitor during parameterization. The interface will also output framing error information, but actions on these errors are prevented.

1+1 Protection

Interfaces 1 and 2 can be 1+1 protected by each other. In protected mode both channels must have the same speed and framing mode settings. A unit working in the protected mode will look like a cross-connect port towards the X-bus. In the protected mode both channels transmit the same data signal coming from a buffer. Both channels use their own frame mux to create the frame structure. The receiving direction includes a change-over switch that selects the active receiver. Rx signal faults are classified into several categories. The switch uses fault categories to select the interface to be used. The fault categories are indicated in the fault table. For example 1.x means the first category (the worst or the most serious fault).

The operating modes of the change-over switch are:

— normal operation
— preferred operation
— forced operation

In the normal operating mode the switch will automatically switch to the other interface if the Rx signal fault category (1, 2, 3, 4, 5, OK) of the active interface continuously is worse than the fault category of the other interface, for a longer period than the given time delay. No switchover operation is activated when the categories are equal for both interfaces.

In the preferred operating mode a switch-over is triggered if there is a difference between the interface fault categories; the better interface is switched active. In a situation with equal fault categories for both interfaces the switch selects the preferred interface.

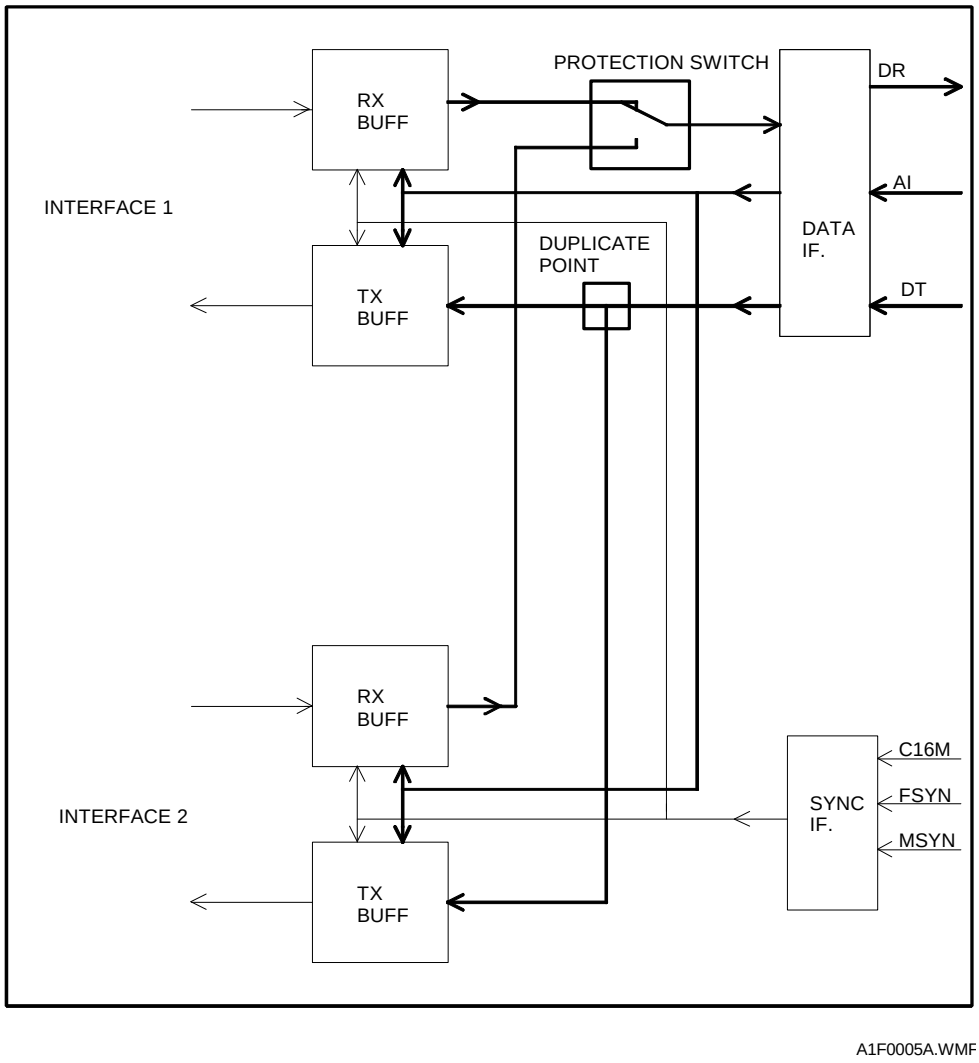


Fig. 48: Block Diagram of Protection

In forced operating mode the switch is forced to switch over without delay. Received data from the active interface is immediately connected to the X-bus. In this situation the Protection switch forced fault message with status MEI appears, and the red LED is turned on.

A switch operating time delay is defined for the prefer operating mode and the normal operating mode. The delay is defined as n x 10 ms, where n=0…6000; i.e. the delay is 0…1 minutes. The delay defines the allowed fault duration before the switch is triggered to switch over.

Fault and Service Status (PMA, DMA, MEI, S) in 1+1 Mode

In principle both interfaces generate their own alarms (alarm messages with fault status). PMA and S statuses are processed in this mode.

PMA Status Processing:

In the protection mode the normal PMA status is changed to the DMA status and there is an additional fault condition, Loss of protected signal, with a PMA status. In normal or preferred operating modes this special condition is created when both interfaces have a fault with fault category 3 or worse. In the forced operating mode this condition occurs if the forced interface has a fault with fault category 3 through 1. The inactive interface is not able to generate a fault with the PMA status.

S Status Processing:

In the protection mode an S status is generated only in the Loss of protected signal fault condition.

Far-End Alarms in 1+1 Mode

A far-end alarm indicates that the Rx signal is out of service (S status)

FrFEA	= Rx frame out of service
MFrFEA	= Rx multiframe out of service

Tx far-end alarms (FrFEA, MFrFEA) of both interfaces are generated assuming a fault status of the active interface. During a short period, when the change-over switch is in a transition phase, the far-end may generate an alarm even if there is no fault in the better interface. In forced operating mode only the active forced interface can cause far-end alarms to be sent.

RxAIS Processing

RxAIS and RxAIS to SigTS are always generated when FAE or MFrFAE is sent. AIS generating depends on the fault status of the selected interface.

Loops in G703-75/120-4CH interface module

The NMS is able to control several loops in the G703-75/120-4CH interface module. Loops and measurement points are used to find a faulty section of the line and to detect the faulty transmitting or receiving direction. The unit includes a loop time-out control which will turn off a loop when the user defined time has come to an end.

Interface Loop

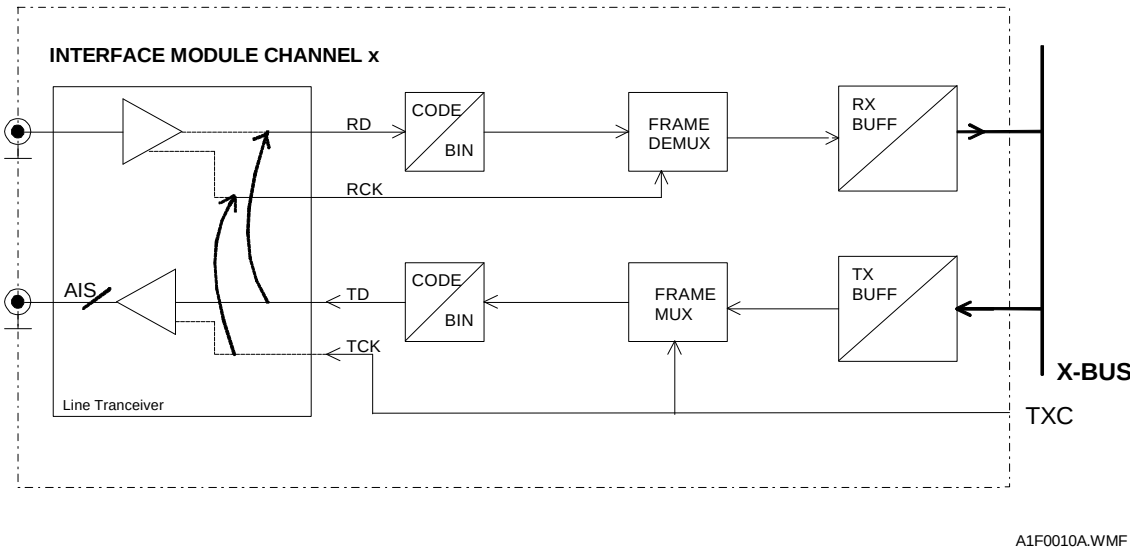


Fig. 49: Interface Loop

An interface loop is created in the interface tranceiver. It loops the transmit data and the clock signal back to the interface receiver. AIS is sent from the interface and the yellow alarm LED is switched on.

Equipment Loop

In an equipment loop the transmit data from the G.704 multiplexer before the line coder/decoder is looped back to the demultiplexer. The interface sends an AIS and the yellow alarm LED is switched on.

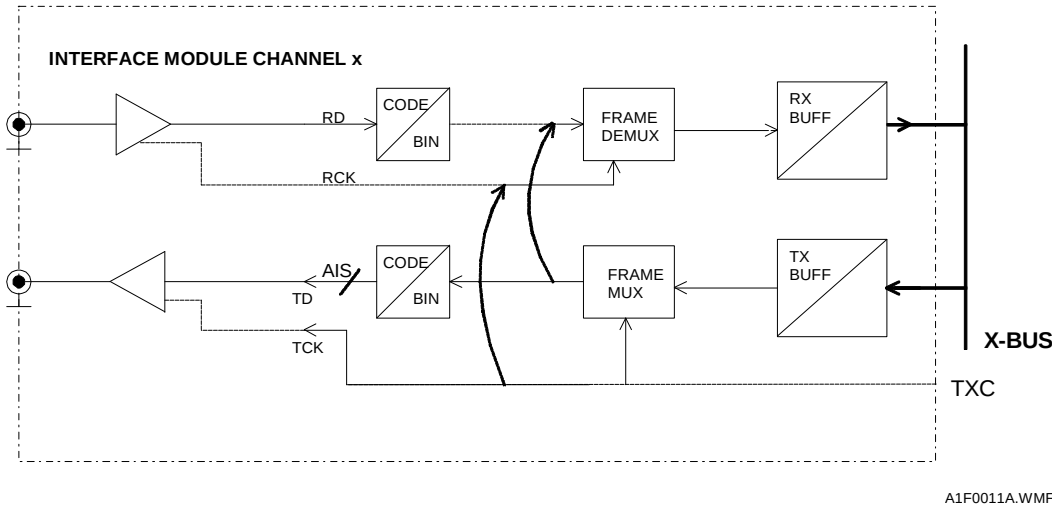


Fig. 50: Equipment Loop

This loop tests the frame multiplexer and demultiplexer. Neither the line coder/decoder nor the interface transceiver are included in the loop. It is also possible to detect faults in the transmitting and receiving buffers when a test signal from a measurement equipment is added to the signal passing through the looped channel. If no problems are detected with the interface loop, it is suggested to perform a test with the equipment loop to ensure that the module is in order.

Line Loop

In the line loop the Rx data received by the interface module is looped back to the interface transmitter. The received clock signal is used as the transmitter clock. AIS is connected to the X-bus instead of the received signal. The yellow alarm LED is switched on.

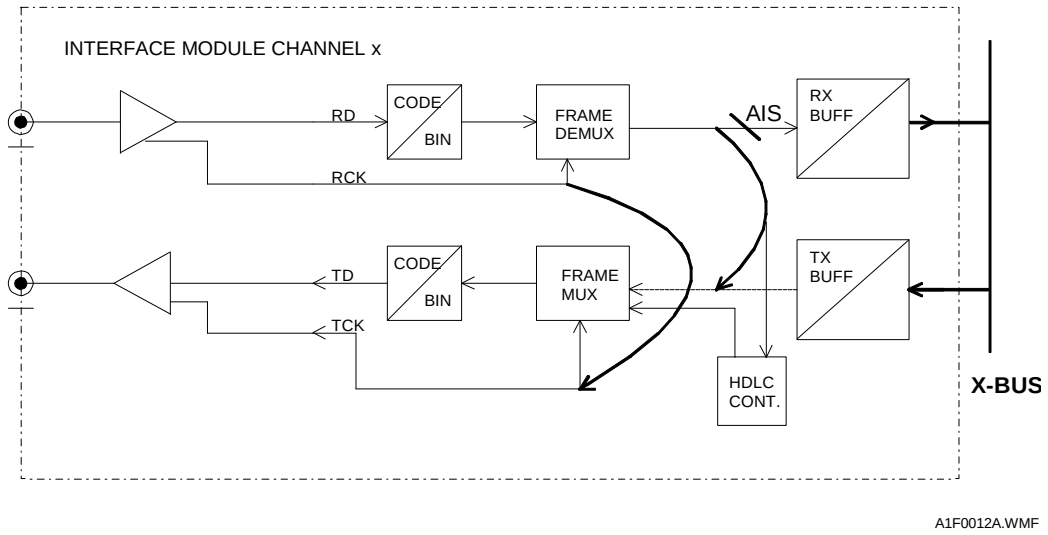


Fig. 51: Line Loop

The interface module, line coder and decoder as well as the frame demultiplexer and multiplexer can be tested from the module's line connector with the Line Loop Test. When it is used, the HDLC controller works with the line loop. All other bits are looped back to the interface.

Remote Line Loop

The remote line loop operates in the looped unit in the same way as the (local) line loop. The remote line loop is activated from the unit at the other end of the line. The loop is made via the HDLC channel and the control channel continues to operate even when the remote line loop is active. The status of the looped unit can be checked with the service computer. When the loop is made, the yellow LED of the unit which controls the loop is switched on, and the yellow LED of the looped unit is also switched on. The whole line can be tested with the remote line loop.

Clock RAI

The interface module can employ a dedicated bit of the frame structure as a far-end clock alarm bit. When a node loses the synchronization with the network, it activates the alarm bit. When the node receiving synchronization from the faulted node detects the alarm state of this bit, it can cease to use the corrupted clock and select the next clock source from the fallback list.

The NMS is able to select the bit used as a clock RAI. The user must choose a time slot and a bit for the clock RAI. The clock RAI time slot cannot be used for payload data. Special bits like HDLC can, however, be used in the same time slot with the clock RAI. The user must also select the polarity (active state).

The interface activates the clock RAI in the transmitting direction when it receives an alarm message from the cross-connect unit via the control bus. The clock RAI is inactivated in a corresponding manner.

In the Rx direction the clock RAI bit is separated from the incoming data and sampled by the processor with a sampling period of about 10 ms. The state of the bit is preserved when two consecutive equal states are detected. When a unit in the active state receives the clock RAI bit, it will cut off the SYB clock if it has one. If the cross-connect unit loses the SYB clock, it will select the next clock source in the fallback list. If the clock signal is lost for a short period, the interface module returns the clock to the SYB bus when the clock RAI is inactivated and then the cross-connect unit again will use the clock. If the synchronization is lost for a longer period, the cross-connect unit will remove the faulted interface from the SYB bus by a command through the control bus; thereafter the cross-connect unit directs a command to the next object in the fallback list without an SYB bus to have it connect the clock to the cleared SYB line.

G703-75/120-4CH Interface Module Front Panel

The module front panel houses two alarm LEDs, four channel interfaces and a synchronization interface which is of the same type as the channel interfaces. Service computer interface is located in XCG base unit.

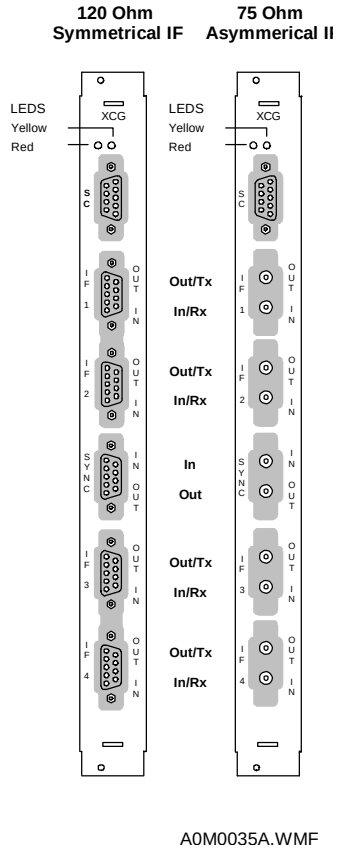


Fig. 52: G703-75/120-4CH modules installed in XCG base unit

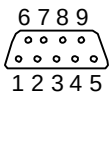
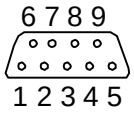


Fig. 53: 120 Ω balanced line interface (IF 1…4) connector pinout

Pin Usage for 120 Ω balanced line interface IF1-4 connector D9 Female

Pin	Signal
1	TxA
2	TxB
3, 6…9	GND
4	RxA
5	RxB

G703-75-4CH channel interface coaxial connector positions are shown in Fig. 52.



A1C0001A.WMF

Fig. 54: 120 Ω balanced SYNC interface connector pinout

Pin Usage for 120 Ω balanced SYNC interface connector pinout D9 Female

Pin	Signal
1	Input A
2	Input B
3, 6…9	GND
4	Output A
5	Output B

G703-75-4CH SYNC interface coaxial connector positions are shown in Fig. 52.

G703-75/120-4CH Module Technical Specifications

Frame and Multiframe Operation

Filtering of FEA and MFrFEA bit:

The state of the alarm bit will switch if the opposite state is received three times consecutively.

AIS in frame 2048 kbit/s:

Signal containing two or less zeroes in a 2-frame period is recognized as an AIS signal. After AIS is detected, a signal containing three or more zeroes in a 2-frame period is recognized not to be an AIS signal.

AIS in multiframe:

A signal in the signalling time slots containing one or no zeroes in a multiframe period is recognized as an AIS signal.

Error rate 10E-3 limits from frame alignment word:

2048 kbit/s, Count time is four seconds	
Count to activate alarm:	94
Count to inactivate alarm:	17

Error rate 10E-3 limits from code errors:

2048 kbit/s, Count time is one second	
Count to activate alarm:	1973
Count to inactivate alarm:	229

CRC spurious frame alignment limits:

2048 kbit/s	915

Power requirement

GDH 522/521	3,5 W

Mechanics

Weight

GDH 521	250 gr
GDH 522	252 gr

Module dimensions: 20 x 135 x 228 mm

Line Interfaces

Nominal impedance	**75 Ω unbalanced/GDH 521**	**120 Ω unbalanced/GDH 522**
Bit rate	2048 kbit/s ± 50 ppm	2048 kbit/s ± 50 ppm
Code	HDB3 (G.703 Annex A)	HDB3 (G.703 Annex A)
Pulse shape	G.703 figure 15	G.703 figure 15
Nominal peak voltage	2.37 V	3.0 V
Nominal pulse width	244 ± 25 ns	244 ± 25 ns
Attenuation margin	6 dB at 1024 kHz	6 dB at 1024 kHz
Input return loss	G.703 § 6.3.3	G.703 § 6.3.3
Output return loss	ETS 300 166 § 5.3	ETS 300 166 § 5.3
Jitter tolerance	G.823 § 3.1.1	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the XCG operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)	< 0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from any 2.048 Mbit/s G.703 interface or XCG external Clock input interface	TBR 12 § 5.2.1.4 TBR 13 § 5.2.1.4	TBR 12 § 5.2.1.4 TBR 13 § 5.2.1.4
Output short circuit current	< 50mA RMS (75Ω)	
Connector type	SMB	D-type 9-pin female connector
Overvoltage Protection	G.703 Annex B	G.703 Annex B

External Clock Input Interface (G.703 § 10.3)

Impedance	75Ω coaxial (GDH 521) or 120Ω symmetrical (GDH 522)
Nominal frequency	N x 64 kHz; N = 1…132
Frequency tolerance	± 50 ppm
Connector	SMB-connector male or 9-pin D-connector female
Input attenuation	6 dB at 2048 kHz max. relative to the output pulse
Return loss	15 dB min. at 2048 kHz
Over voltage protection	G.703 Annex B
Continuous signal level	5 V rms max.
Grounding	Cable shields are grounded

Node Clock Output Interface (G.703 § 10.2)

Impedance	75Ω coaxial (GDH 521) or 120 Ω symmetrical (GDH 522)
Connector	SMB-connector male or 9-pin D-connector female
Output pulse at 2048 kHz	see (G.703 § 10.2)
Pulse amplitude	V min = 0.75 V, V max. = 1.5 V at 75 Ω V min = 1.0 V, V max. = 1.9 V at 120 Ω
Nominal frequency	8448, 2048, 1408, 1024, 768, 704, 512, 384, 256, 192, 128, 64 kHz
Over voltage protection	G.703 Annex B
Grounding	Cable shields are grounded

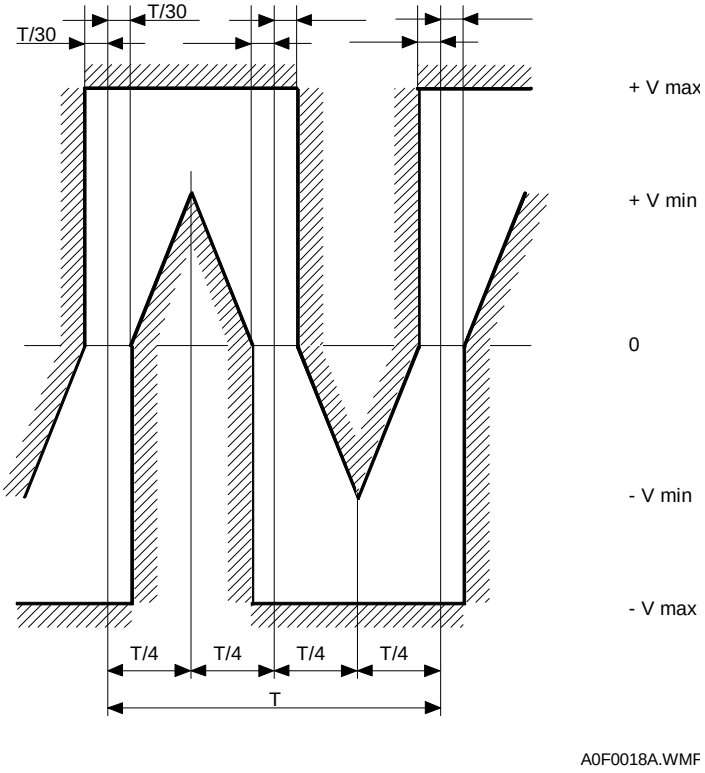


Fig. 55: Clock Output Pulse Mask at 2048 kHz

Jitter transfer function from 2 Mbit/s port A to 2 Mbit/s port B or from an external clock at 2048 kHz to a 2 Mbit/s port

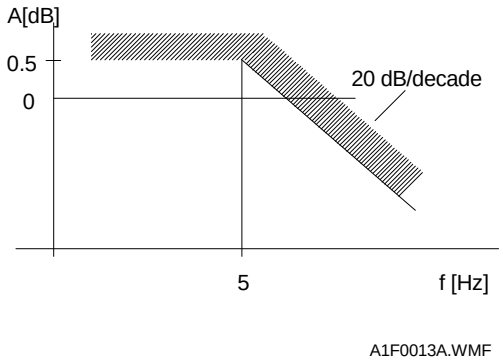


Fig. 56: Jitter Transfer Function

2.7.3 Faults and Actions

2.7.3.1 Terminology

The acronyms explained below will be used in the following tables:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Alarm
R = Red alarm LED
Y = Yellow alarm LED
RB = Red alarm LED blink
TxAIS = AIS insertion to Tx signal
RxAIS = AIS insertion to Rx signal
TxTS-AIS = AIS insertion in time slots of Tx signal
FrFEA = Frame level far-end alarm (ts0/B3 in 2Mbit/s frame)
MFrFEA = Multiframe level far-end alarm (FR0/ta sig/B6)
MFrFEA is also transmitted if FrFEA is transmitted.

2.7.3.2 XCG Faults

Fault Condition	Status	LED	Note
Reset of Unit	PMA	R	

Power Supply Faults

Fault Condition	Status	LED	Note
Power + 5 V	PMA	R	
Power + 12 V	PMA	R	
Power - 10 V	PMA	R	

Memory Faults

Fault Condition	Status	LED	Note
RAM Fault	PMA	R	
EPROM Fault	PMA	R	
Flash Write Error	PMA	R	
Flash Copy Error	PMA	R	
Flash Erase Error	PMA	R	
Flash Dublicate Error	PMA	R	
Flash Shadow Error	PMA	R	
Flash Check Sum Error	PMA, S	R	
Missing Settings	PMA	R	
Incompatible SW in EPROM and FLASH	PMA	R	

Cross-Connection Faults

Fault Condition	Status	LED	Note
X-Connect RAM Fault	PMA, S	R	
Block 1/2/3/4 IA Fault	PMA, S	Y	
Loss of Master Clock Locking	MEI		
Fallback list Warning	MEI		
Loss of External Clock	PMA,	R	
Phase Locked Loop Alarm	PMA	R	
External Clock Warning	MEI		
Clock Far End Alarm of Choice 1/2/3/4/5	MEI	Y	
Flash List Check Sum Error	PMA, S	R	
ASIC Latch Error	PMA, S	R	
ASIC Latch Warning	MEI		
Time Controlled X-connect Warning	PMA		
X-Connect Flash List Conflict	MEI		
PortDesc Flash List Conflict	MEI		
Swapped Trunk Flash List Conflict	MEI		
Passivated Trunk Flash List Conflict	MEI		
Unit IA Fault	PMA, S	Y	
Inventory Faults			
Missing Unit	PMA, S	Y	Service alarm
Extra Unit	MEI	Y	

2.7.3.3 G703-75/120-4CH Interface Module Faults and Actions

Tx Signal Faults (Block 1, 2, 3, 4)

Fault Condition	Status	LED	Tx signal
Tx Clock fault (PLL)	PMA, S	R	TxAIS
Bus faults IA activity missing Bus sync. fault (block 0)	 PMA, S PMA, S	 R Y	 TxTS-AIS TxTS-AIS
AIS from X-bus	MEI, S	Y	TxAIS[a]

a Only when FAS is transferred through the network

Rx Signal Faults (Block 1, 2, 3, 4)

Signal & Frame Faults	Status	LED	Rx signal	Tx signal
1.1 Rx signal missing	PMA, S	R	RxAIS	FrFEA
1.2 Rx signal is AIS	MEI, S	Y	RxAIS	FrFEA
1.3 Loss of frame alignment 1.3.1 Frame alignment lost 1.3.3 Frame alignment lost by CRC -> 915/1000 errored CRC-blocks 1.3.2 CRC missing	 PMA, S PMA, S DMA	 R R R	 RxAIS RxAIS RxAIS	 FrFEA FrFEA FrFEA
1.4 BER 10-3 - frame alignment word (normal error response) - line code errors - n x 64 kbit/s baseband signal	PMA, S	R	RxAIS	FrFEA
1.5 Wrong input signal 1.5.1 Own NNM messages received 1.5.2 Wrong IDs in NNM messages (detection can be inhibited) 1.5.3 No response to NNM message	 PMA, S PMA, S PMA, S	 R R R	 RxAIS RxAIS RxAIS	 - - -
1.6 ASIC register error	PMA, S	R	-	-
Loops	Status	LED	Rx signal	Tx Signal
2.1 Local loops 2.1.1 Interface back to equipment 2.1.2 MUX/DEMUX back to eq. 2.1.3 MUX/DEMUX back to line 2.1.4 Line loop made by neighbour	 MEI, S MEI, S MEI, S MEI, S	 Y Y Y Y	 - - RxAIS RxAIS	 TxAIS TxAIS - -
2.2 Remote loops 2.2.1 Remote controlled line loop	MEI, S	Y	-	-
Multiframe level faults				
3.1 Multiframe alignment lost (group N)	PMA, S	R	RxAIS/ SigTS	MFrFEA
3.2 AIS in signalling (group N)	MEI, S	Y	RxAIS/ SigTS	MFrFEA
Far-end alarms	Status	LED	Rx signal	Note
4.1 Frame far-end alarm (FrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
4.2 Multiframe far-end alarm (MFrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off

Rx Signal Faults (Block 1, 2, 3, 4)

Signal & Frame Faults	Status	LED	Rx signal	Tx signal
Degraded signal	Status	LED	RxAIS	FrFEA
5.1 Error rate 10-3 - frame alignment word (AIS insertion inhibited)	DMA	R	-	-
5.2 Error rate 10-6 - CRC block errors - line code errors	DMA	R	-	-
5.3 Frequency difference - excessive phase drift in input buffer	DMA	R	-	-
5.4 Buffer slips/1 hour	MEI	RB	-	-

Miscellaneous Faults (Block 1, 2)

Fault Condition	Status	LED	Rx signal	Tx signal
Port locking conflict	DMA	R	-	-
HDLC overlap with X-bus	DMA	R	-	-
Master clock RAI overlap with X-bus	DMA	R	-	-
G821 unavailable state	PMA, S	-	-	-
G821 limit event	DMA	-	-	-
Faults masked/Test	MEI	Y	-	-

1+1 Protection Switch Fault Messages (Block 0)

Fault Condition	Status	LED	Rx signal	Tx signal
Protection switch forced	MEI	R	-	-
Loss of protected signal	PMA, S	R	-[a]	-[a]

a Only when FAS is transferred through the network.

2.7.4 XCG Front Panel

Following figure shows the connector locations and the LEDs. 75 Ω asymmetrical interface and 120 Ω symmetrical interface versions are available.

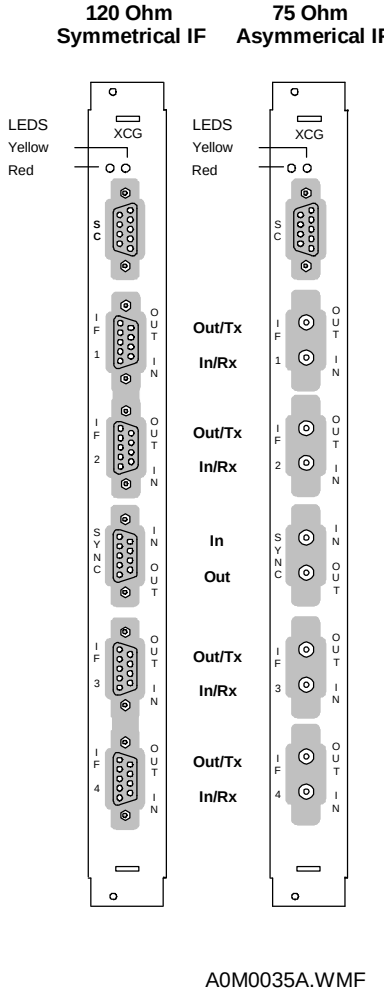


Fig. 57: G703-75/120-4CH interface modules installed in the XCG base unit

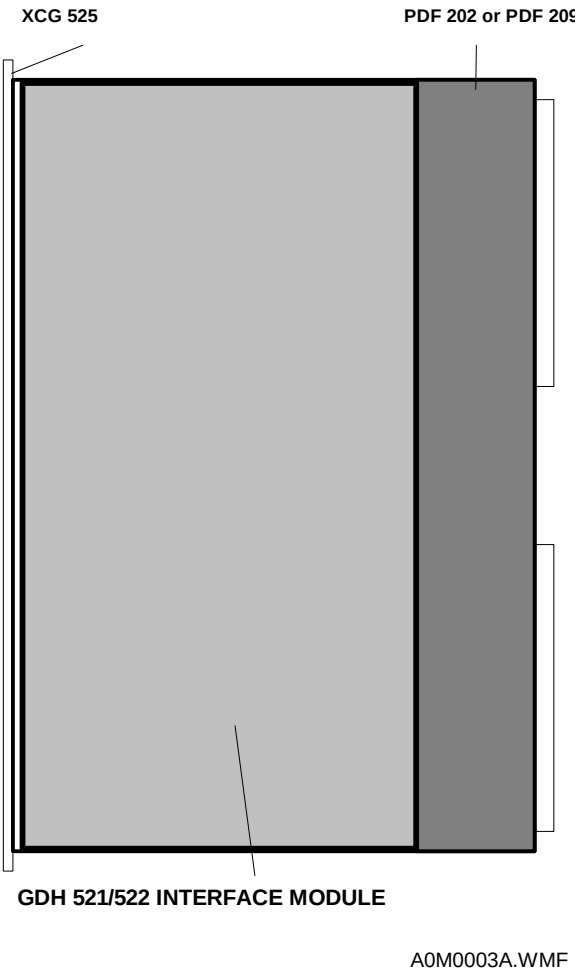


Fig. 58: XCG base unit

2.7.5 XCG Technical Specifications

Cross-Connect

Cross-connection method	**Synchronous time slot interleaving**
Frame frequency	8 kHz
Capacity: The sum of cross-connected signals	64 Mbit/s
Smallest cross-connect unit	8 kbit/s
Signalling cross-connection (XD)	n x 500 bit/s (CAS)
Delay of cross-connect core:	1 frame = 125 µs 2ms n x 64 kbit/s CAS-bits (500 bit/s)
Time integrity between time slots in cross-connected signals is maintained	
CAS TS capacity	= 32 bus time slots
n x 8 kbit/s cross-connect port capacity	= 95 bus time slots

Timing

Master clock frequency	16 896 kHz ± 30 ppm
Master clock functional modes	Locking to the IF rx clock (n x 64 kbit/s) n = 1 to 32
	Locking to external clock input (n x 64 kHz)
	Clock fallback list (5 levels + internal mode)
Frame sync.	8 kHz (125 us)
Multiframe sync (E1)	500 Hz (2ms)
Multiframe sync (T1)	166.66 Hz (6 ms)
Locking frequency	n x 64 kHz ±- 50 ppm
External clock input	n x 64 kHz (n = 1…32) ± 50 ppm
	Electrically G.703 (120 / 75 Ω)
External clock output	2048 kHz ± 30 ppm (Locked to master clock)
	Electrically G.703 (120 / 75 Ω)
Jitter transfer function and jitter in the output	G.736, G.823

The 16.896 Mhz clock is used to generate the main clock for whole node.

Control Interface Specifications

Service Computer Interface	
Purpose	Management interface for SC/NMS
Electrical interface	V.28
Data bit rate	9600 b/s asynchronous
Character format	8 bit, no parity, 1 stop bit
Connector type	D-type 9-pin female connector
Interface signals	102,103,104,105,106,107,108 and 109
Protocol	Layers 2…7 proprietary

Node Clock Jitter and Wander

Output jitter, measured within the frequency range 20 Hz to 100 kHz	
2 Mbit/s and clock port output, internal timing	0.05 UIp-p max.
2 Mbit/s port output, node synchronized from an external clock at 2048 kHz containing no jitter	0.05 UIp-p max.
2 Mbit/s port output, node synchronized from an interface at 2 Mbit/s containing no jitter	0.10 UIp-p max.

Input jitter tolerance at the external clock interface at 2048 kHz

See following figure: (G.823 fig. 3)

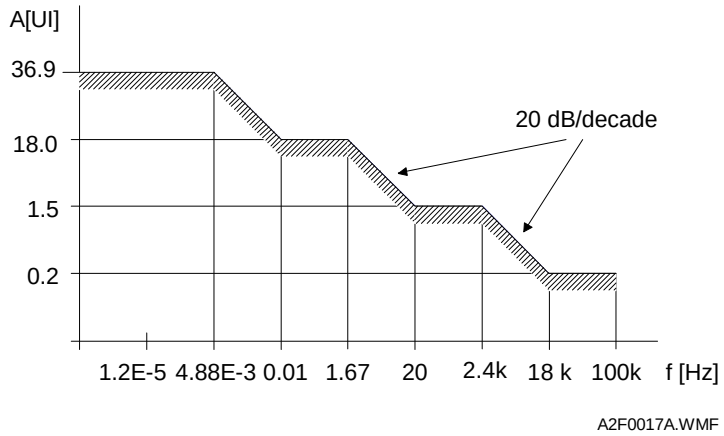


Fig. 59: Input Jitter Tolerance for the External Clock

Jitter transfer function from 2 Mbit/s port A to 2 Mbit/s port B or from an external clock at 2048 kHz to a 2 Mbit/s port

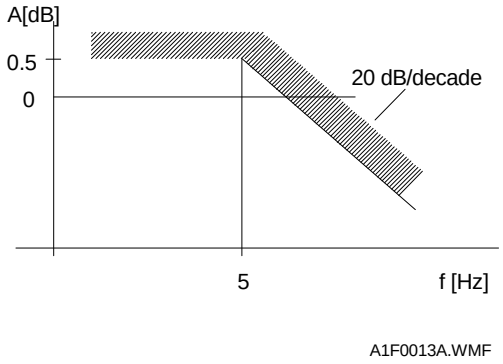


Fig. 60: Jitter Transfer Function